FPGA-Based Algorithm of a High Accuracy Digital TAC

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Introduction

In nuclear structure experiments, the slow-fast technique is used to study coincident gamma rays. The conventional analog electronics setup for this type of coincidence measurement becomes extremely complex for large number of detectors. FPGA based systems provide an efficient and flexible solution for generation of coincidence trigger for such a complex detector array. A FPGA-based algorithm has been developed to accurately measure the time interval between two events in this technique with a worst case error of 2.5ns.

Information related to the timing and energy of the gamma rays help in the study of nuclear reactions. The slow-fast technique is a standard coincidence technique used which utilize two channels to process information. The information about timing is obtained by the fast channel and that for energy by the slow channel in the time window provided by the former. The TAC (Time to Amplitude Converter) provides the time window to the slow circuit. It measures the time elapsed between the start event and the stop event (with an added delay).

Need for a Flexible System

The system used generally is based on analog electronics and is a stand-alone system for two detectors. In actual nuclear structure experiments, one needs to design the coincidence circuit for large number of detectors and the complexity increases exponentially with the increase in the channel number. The FPGA board used (SPARTAN III) has 144 input/output channels which can enable the use of hundreds of detectors simultaneously. Since it is a programmable module, one can make changes in the parameters at any time without disturbing the setup or experiment using remote computing.

Vernier Method of Timing Measurement

The time between the two events, start and stop, are required to be measured accurately to define the coincident event. These measurements have been taken by using Vernier method [1].

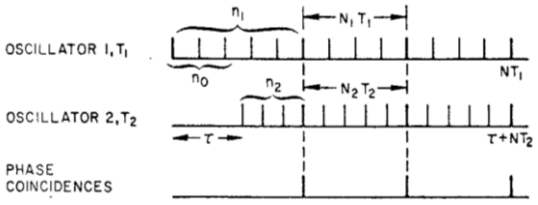

Fig.1. Vernier method [1] for the calculation of time interval between the two events, start and stop is shown. The formula is

$$\tau = N_1 T_1 - N_2 T_2$$

All the operations were synchronised with the system clock of 100MHz. A Digital Clock Manager (DCM) has been used to derive the second clock of slightly different frequency from the system clock. A counter starts counting at the next rising edge of the clock pulse after it is enabled by the start/ stop pulse. Hence the maximum possible error at the start of each counter is equal to one clock period as illustrated:

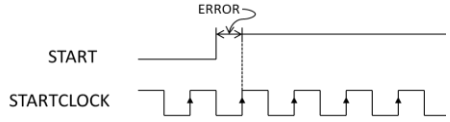

Fig. 2. The error due to the mismatch between the rising edge of startclock and start pulse is shown.

F.P.G.A.-Based Algorithm for Minimizing the Worst-Case Error

The maximum error here is 10ns and the maximum total error is 20ns (start and stop). To reduce the error, the clock frequency is doubled with a DCM as the maximum frequency with which the given board can work is 200MHz reducing the maximum total error to 10ns.

The clock is phase shifted simultaneously (0 , 90, 180, 270) to give four clocks of same frequency but with the rising edge occuring four times in a given span of 5ns (the new time period). A logic is developed such that the clock which has the rising edge closest to the start pulse is selected as final clock which is used by the start counter. Also, we have four stop clocks of slightly different frequency from start clocks, again phase shifted. The same procedure is followed for trigerring the stop counter when the stop pulse arrives and the Vernier Method is applied.

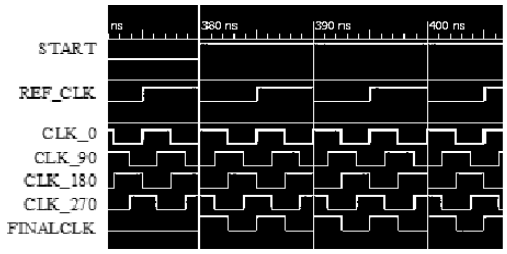

Fig.3. In this case the rising edge of CLK_0 is nearest to the rising edge of the start event. The FINALCLK is equivalent to the CLK_0.

Thus the error is reduced to 1.25ns for each start and stop count. However, the probability of maximum error occuring at both the start and stop count in such a way that it adds up to 2.5ns is extremely small. Ordinarily the error is within 1ns.

Simulation and Results

In the coincidence setup, a fixed delay (here 200ns) is given to one of the coincident signals and the final time difference is measured. However, due to the intermediate instruments used, the actual time difference varies as a gaussian distribution with mean at 200ns. For simulation using Xilinx ISim two data sets were taken and the simulation was tested for 40 randomely generated data points ranging from 190ns to 210ns. The results are plotted as a Gaussian distribution using MATLAB as shown in Fig.4.

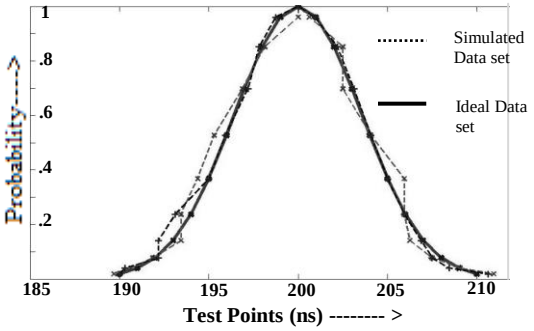

Fig.4 The graph shows how close the simulated data lies compared to the ideal data. The test points (time differences) are plotted on the x-axis and their probability distribution as a Gaussian function is plotted as weight factors on the y- axis.

The error ranged from .06ns to 1ns in the given sample.Thus it is possible to achieve avaerage error less than one nanosecond and worst case error equal to 2.5ns.

Future Work

The accuracy can be further improved by phase shifting the clock by smaller amounts using delay elements of sub-ns intervals. Therefore, the worst case error will range in ps [2]. This technique needs to be implemented on F.P.G.A. board and tested in the actual experimental setup.

Acknowledgements

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References

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[2] Jansson Jussi-Pekka, Mäntyniemi Antti, Kostamovaara Juha, A CMOS Time-to-Digital Converter with Better than 10ps Single – Shot Precision, IEEE Journal of Solid-State Circuits, Vol. 41, No. 6, June 2006