Low Voltage Distribution Board (LVDB) for ALICE Photon Multiplicity Detector

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Introduction

The readout of the A Large Ion Collider Experiment (ALICE) - Photon Multiplicity Detector (PMD) [2] involves reading of 221184 channels. These channels are distributed among 48 detector modules with each module having 4608 channels. The readout is organized in chains with each chain reading 12 Front End Electronics (FEE) boards (768 channels) using one translator board. Therefore each detector module is organized in 6 readout chains. Each FEE board reads 64 channels with 4 Multiplexed ANAlog Signal Processor (MANAS) chips and each MANAS reading 16 channels. The low voltage required for these readout chains are +/- 2.5V (VDD, VSS) for analog circuits and +3.3V (VCC) for digital circuits. PMD is a gas detector with HV of 1400V. The readout being wire read out, the anode wire is directly coupled to the inputs of the front end chips i.e. MANAS on the on the FEE boards which goes bad, drawing huge currents leading to over current in the FEE board which may result in LV trips. So it is required to protect readout chain against over current and at the same time achieve Low voltage segmentation to isolate the tripped chain from working chain at the time of data run.

Low Voltage Distribution Board (LVDB) is designed to feed power to readout chains. The LVDB has 6 channels with each channel having +/- 2.5 and +3.3V. These 6 channels provide low voltage to 6 chains of one PMD module. It has Low voltage segmentation chain wise which trips the LV (+/-2.5V) of a faulty chain in a over current situation and LV to all other readout chains of the module is unaffected. The faulty chain can be recovered by resetting if the fault is momentary. Each LVDB is powered by 3 low voltage channels at the inputs from the low voltage modules of CAEN (EASY 3000 series) which are installed 40meter away from the detector. LVDB reduces LV channels of power supply and cabling from detector to power supply racks by factor of 6, which was not practical and even very costly. The LVDB has over current protection feature for the analog circuitry i.e. +/- 2.5V required for MANAS chips and not for the digital circuits. There was no protection for +3.3V due to Data Acquisition System (DAQ) requirements, it was seen that due to long distance cable of LV, power glitches occurring during the On and OFF of the LV power supply, LVDS components of FEE boards were going bad which were getting power with +3.3V line. So a Transient Voltage Suppressor (TVS) diode was introduced in +3.3V line on LVDB to protect FEE from unwanted power glitches.

The LVDB was to be installed and operated in high magnetic field and a confined area with no cooling facility. Therefore a circuit was designed with very low power dissipation of only 200mW on LVDB with load requirements of -2.5V/7A, +2.5V/5.5A and +3.3V/3.5A. For this, a MOS based design was adopted instead of an electromagnetic relays unlike earlier designs used in STAR-PMD[1] at BNL. The advantages are (1) Electromagnetic relays are bulky and can't be used due to severe space limitations. (2)They can't be used in magnetic field environment. (3) They are very slow. (4) Contact resistances are high causing more voltage drops. (5) They are mechanical switches, so they are prone to contact problem. The board was installed in high radiation environment. So the components were chosen to be able to work in such environment. Radiation hardness tests were done at RRCAT Indore and it was found that the entire components of the board were sustaining 24Krad of equivalent radiation. For the test purpose Co_{60} source was used. This radiation hardness of the board was accepted by ALICE technicals for installation in ALICE-PMD environment.

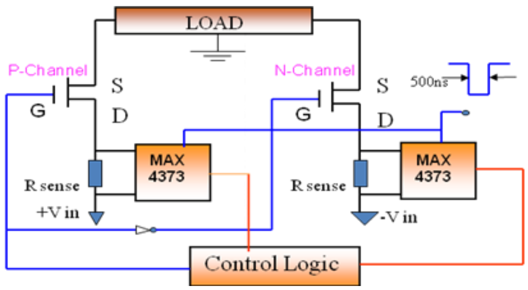

Fig-1 Basic building block of LVDB

Fig.1 shows the basic building block of the low voltage distribution circuit based on MAX4373, sense resistors, control logic and dual channel MOSFET (IRF7338) as switching elements. MAX4373 is a low cost, micro power IC containing high side current sense amplifier, band gap reference and a comparator with latching output. The current sense resistor is coming in series so the resistance should be as low as possible. In this circuit sense resistance is 15mΩ and MAX4373 with 100gain is chosen to sense small change. In this circuit MOSFET'S are used as switching device with the logic IC's to trip in case of over current. This MOS is in series so the on state resistance should be low. For IRF7338, the on state resistance for n-channel is 30mΩ and for p-channel it is 150mΩ. These components ensure low voltage drop and power-dissipation on board.

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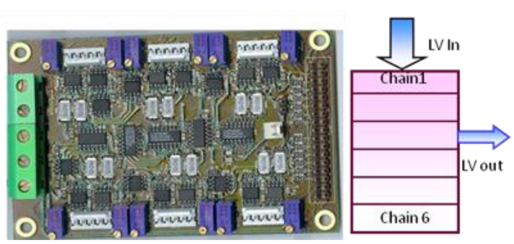

Fig. 2 LVDB picture with supply block diagram

In the ALICE DAQ, once the chain is tripped it should remain tripped till a run is stopped. Before a new run start a RESET can be sent by Detector control system (DCS) to see if the chain recovers from the damage. A remote status monitoring of the channels are also done by DCS coupled with LVDB. This status indicates the health of the readout chain as well as the LVDB fault.

After testing of circuit, schematic was made in ISIS software and layout was made in ARES software taking care of high current requirements of load, which is a 6-layer PCB and after fabrication and assembly in lab, final LVDB can be seen in fig.2. Such 60-boards are assembled and tested in lab. These LVDB are installed and commissioned in the carven of ALICE-PMD, CERN, Geneva and working satisfactorily for last 3-years. The details of the design and test results will be presented.

References

[1] PMD Low voltage power protection and distribution circuit by D. Padrazo, STAR, BNL.

[2] Photon Multiplicity Detector Technical Design Report CERN/LHCC 99-32