A protoype FPGA-based digital pulse processing system

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Abstract:
Data acquisition systems for nuclear physics experiments have traditionally been based on hybrid systems with analog shaping amplifiers followed by analog to digital converters. Recently however new systems based on digital signal processing concepts have been developed. A FPGA based cPCI board with high speed analog inputs has been designed. This board has recently been used to acquire mono energetic alpha pulses from an ^{241}Am source. This paper first, introduces the concept of a digital pulse processing system. Finally the results obtained from the acquired pulses are reported.

Introduction:
Digital pulse processing is a signal processing technique in which detector (preamplifier output) signals are directly digitized and processed to extract quantities of interest. The first stage in a digital pulse processing set-up is signal digitization after pre-amplification (refer figure.1). Once the pulse is digitized it becomes immune to signal distortions due to electronic noise and temperature instabilities. The analyses of the digitized data can then be done in real-time as soon as the pulse is digitized or in a post-processing step on the stored data. Digital signal processing techniques can then be used to extract the desired parameters like pulse shape, height, rise time. DSP based techniques have also been used for particle identification [1].

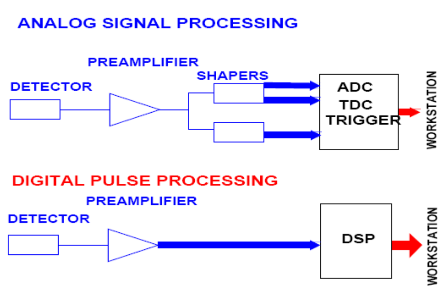

Figure 1: Analog and digital pulse processing systems.

Description:
A FPGA based cPCI board, designed in-house has been used to capture and store mono-energetic alpha pulses ^{241}Am source (refer figure 2). The details of the board are as follows:

- Form factor: 6U.
- FPGA:VIRTEX-5 XC5VFX100T
- cPCI interface: 32 bit, 33MHz master interface with DMA transfer capability using *PCI 9054* from PLX Technology.
- Clock: 156.25 MHz clock oscillator for SFP; 40 MHz clock oscillator for PCI; 32 MHz system clock; Clock distribution for ADC and DAC.
- Rocket IO interface: Two SFP connectors are provided for SFP modules
- Memory: 2GB DDR2 – SDRAM; 256Mb flash Memory
- Analog Input: Two channels using 12 bit, 1.0 GSPS ADC: ADC12D1000 from National Semiconductor
- Configuration: JTAG Mode; Using On-board Configuration *PROM.*

The alpha particles from the source are detected using a silicon strip detector. The signal is amplified and split into two channels. One channel in given to a constant fraction discriminator (CFD) through a timing filter amplifier (TFA). A TTL level trigger pulse is finally generated using this channel. The signal from the second channel is fed to the data acquisition board. This signal is digitized at a rate of 1 Giga samples per second and the digitized data is transferred to the PC through a PCI bus (refer figure 3). The data acquisition design implemented in the FPGA includes pre-triggering, writing and reading data to and from an on-board DDR2 RAM and also interfacing with a 32 bit 33 MHz PCI bus. The system is implemented in a way that data can be analyzed in an off-line mode.

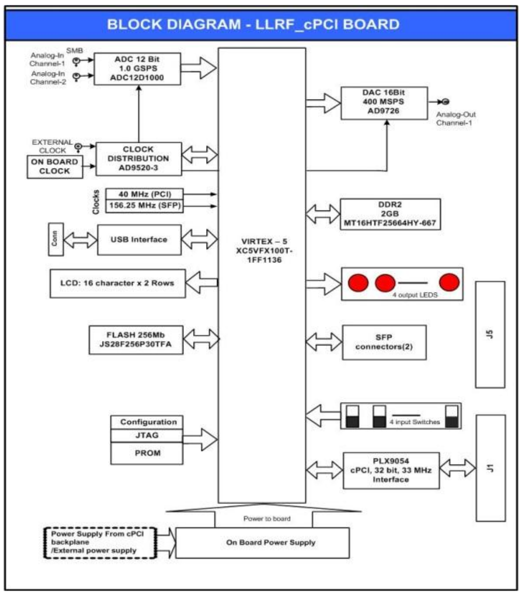

Figure 2: Block diagram of cPCI board

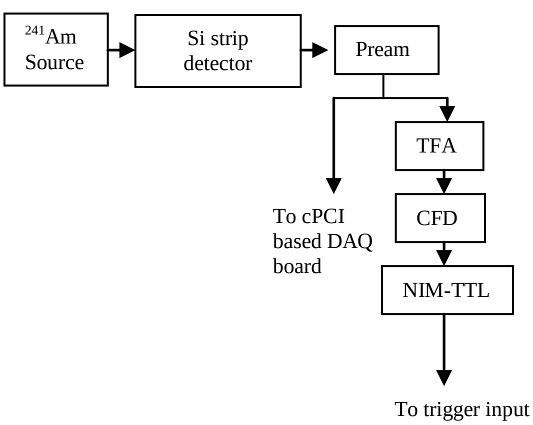

Figure 3: Pulse acquisition schematic

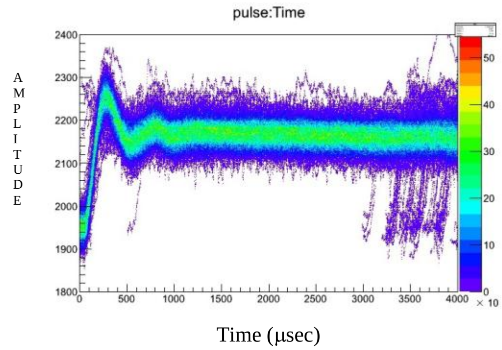

Figure 4: Overlapped pulses acquired from cPCI board

Conclusion and future work:

It has been observed that the pulse height is constant for a sample of 1000 pulses as shown in figure 4. We plan to do similar measurements using Pu-Am and Th sources covering a energy range of 4-9 MeV. From the pulse height, the energy spectra and Full width at Half Maximum will be obtained. This will help in further verifying the board design for use in future digital pulse processing systems.

References:

[1] Identification of light particles by means of pulse shape analysis with silicon detector at low energy.
J.A. Duenas, D. Mengoni, V.V Parkar et al Nuclear Instruments and Methods in Physics Research A 676(2012) 70-73