Silicon Pad Detectors for ALICE Forward Calorimeter

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A newly designed Electromagnetic Calorimeter (EMC) is being proposed as a possible upgrade in the Forward rapidity region,to enhance the physics capabilities of the ALICE experiment at CERN. Each LHC experiment uses a unique approach, in which preference of the designers and the physics requirements has played a decisive role. The requirement of the design of the calorimeter is to have highly granular layers of detectors consisting of 1mm^2 as well as 1cm^2 silicon pad detectors. The high granular layers (1mm^2) yield good position resolution and tracking of incoming particles. Other active layers, composed of pads of 1cm^2 are used for energy measurement.

For full containment of photon energy up to two hundred GeV, it has been found that 25-radiation length (layers) of material is sufficient. For this purpose, a sampling type calorimeter with tungsten as absorber and silicon as active detector material has been considered. Silicon (PIN) pad detectors are preferred for a number of reasons. Silicon PIN detector has no inherent charge gain and intrinsically it is fast. It operates under relatively low bias voltage. The relatively lower sensitivity to magnetic field is another attractive feature of this type of detectors.

The proposed calorimeter will be a novel compact silicon-tungsten sandwich-type design, which will be used for the first time in any high-energy physics experiment. The design of the pad detectors is underway. It is planned to fabricate the silicon pad detector at Bharat Electronics Limited (BEL), Bangalore.

The proposed Electromagnetic Calorimeter will be installed at a distance of about 3.5 meters from the vertex and cover a region of 2.5 to 4.8 in pseudo-rapidity.

In order to get a preliminary knowledge of silicon pad detectors and readout electronics interface, 1cm^2 silicon pad detectors are used for testing. The initial results of the 1cm^2 pad detectors interfaced with conventional electronics, MANAS[1] and also with ASIC ANUSANSKAR[2] designed at ED, BARC are presented here.

Silicon detectors used for testing are of 1cm^2 in area, 320um thick, full depletion voltages of about 70-80 volts with full depletion capacitance of 40pF/cm^2 fabricated and mounted on a ceramic base as shown in Fig.1. The detectors were supplied by BEL and tests were performed at VECC.

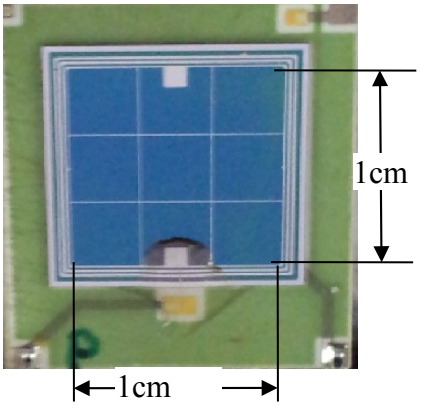

Fig.1 A 1 cm^2 Silicon Pad Detector mounted on a PCB

Fig. 2 shows the biasing scheme [3] for the silicon pad detectors, where detector is the silicon pad and R3, R5 and R6 are the biasing resistors. CAEN N471A HV module is used for biasing. MIP spectra of different Beta Sources are obtained on Multi Channel Analyzer (MCA).

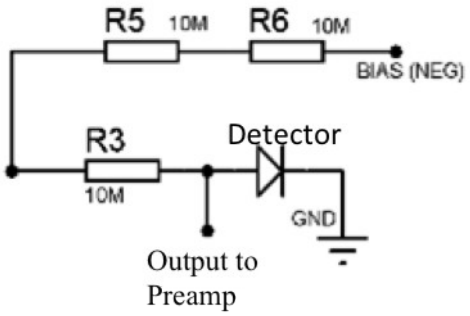

Fig.2 Biasing scheme for silicon pad detector to test with Beta Sources

A bias voltage of 60 volts is applied on silicon PAD detector with a shaping time constant of 0.5 micro-sec in order to observe the Beta spectrum. Separation in individual noise peak and signal peak are clearly distinguishable, with Sr-90 Beta source as shown in Fig 3.

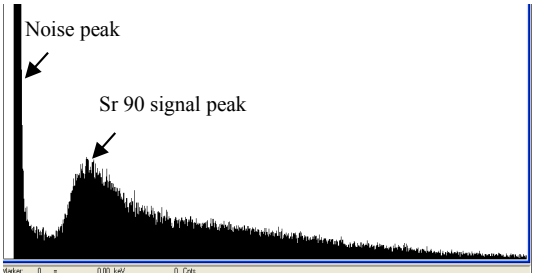

Fig.3 Response of 1cm^2 silicon strip detector to the Beta Sr-90 Source

Further tests are being carried out by varying the bias voltage of the detector, varying the biasing resistance in the biasing scheme, varying the gain and shaping time of the amplifier and with different radioactive sources to find the optimized parameters of the detector.

These silicon pads are also readout with different ASICs such as MANAS, designed for ALICE and ANUSANSKAR. Preliminary test results of ASIC ANUSANSKAR coupled with silicon PAD detector with clear separation (Beta spectrum) between the noise and signal peak is shown in Fig.4.

Fig.4 Beta spectrum of Sr-90 with ANUSANSKAR ASIC coupled with PAD detector

Four PCBs each with an array of 5 x 5 elements (each 1cm^2) silicon pad detectors is designed and being fabricated with minimum dead space between the detector active areas. These PCBs will be put in between tungsten layers and will be coupled with CROCUS DAQ for feasibility study of the calorimeter. These arrays will be tested during the next test beam time at CERN, Geneva. The aim is to study the behavior and characteristics of the detector and requirements of front-end electronics with regards to dynamic range and optimize different parameters. Front End Electronics board using ANUSANSKAR and MARC (used in the ALICE-PMD FEE board) is under design process. The laboratory and beam line test results will be reported in the symposium.

References:

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By Helmuth Speiler. Lecture Notes, ICFA instrumentation school.