Capacitance measurement of Penning trap electrode assembly at cryogenic temperature

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Introduction

Ion traps provide a very clean, virtually background free environment, long sampling times and ultra low particle energy for various high precision measurements. The primary requirement in an ion trap experiment is to diagnose the number of trapped ions continuously and nondestructively. Wineland and Dehment [1] had demonstrated a way to determine the number of trapped charged particles by measuring the separation of two resonant peaks when an external tank circuit is coupled to the centre of mass (CM) motion of the particles in the trap.

In order to determine the number of trapped electrons in the cryogenic Penning Ion trap being developed at VECC, we are planning to build a tank circuit. As the tank circuit would be coupled to electrons trapped by the five electrode othrogonalized trapping arrangement, determination of the capacitance of the five electrode trap arrangement is an essential requirement. We report here the measurement technique developed for accurate determination of capacitance of the trap assembly at cryogenic temperature using Colpitts oscillator operating at room temperature. For this purpose a cryogenic setup with two temperature regions has been designed for the capacitance measurement using the scheme described below.

Measurement Scheme

Since, the axial frequency of the trapped electrons in the cryogenic Penning trap (5 Tesla magnetic field and potentials applied to the five electrode trap assembly) would be ~63 MHz, a Colpitts Oscillator has been designed to operate near 63 MHz shown in Fig.1(a). A feedback signal for oscillation is taken from a voltage divider made by two capacitors ‘C5’ and ‘C6’. The second stage is a buffer circuit from Texas Instruments (BUF 602) which gives a 50Ω drive output for the transmission line. A 7th order Butterworth low pass filter is designed for suppressing higher order harmonics. In this configuration, ‘C’ is the unknown capacitance to be measured. The circuit designed and developed is shown in Fig 1(b).

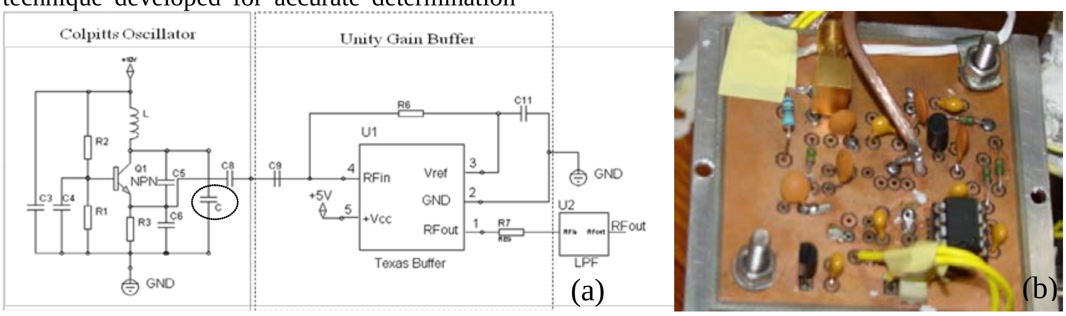

Fig.1: Colpitts Oscillator followed by a unity gain buffer and Low pass filter

Calibration and measurement at RT

Colpitts oscillator circuit was used to measure capacitance by recording the oscillation frequency f_1 (without capacitance) and f_2 (with capacitance "C" as shown in Fig1a) following the method given below

$$f_1 = \frac{1}{2\pi\sqrt{LC_{eq}}}, \; f_2 = \frac{1}{2\pi\sqrt{L(C_{eq}+C)}} \qquad (1)$$

$$C = C_{eq}\left(\frac{f_1}{f_2}\right)^2 - C_{eq} = C_{eq}F - C_{eq} \qquad (2)$$

Where, $F = \left(f_1 / f_2 \right)^2$

The calibration was done by measuring different standard capacitance (0.5pF – 10pF) in the capacitance slot of the above circuit and its response has been plotted in Fig 2.

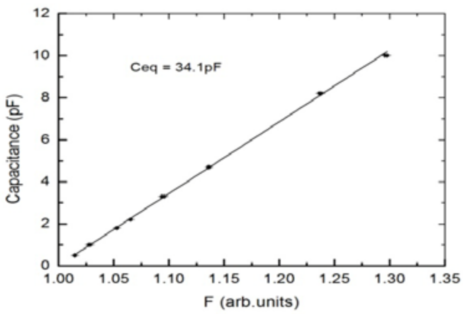

Fig. 2.: C-F response of the Colpitts Oscillator

Trap capacitance measurement

Trap Capacitance was determined at Room Temperature by connecting the trap electrodes pins to the capacitor (C) slot with two short wires using the scheme mentioned above. The measured value was found to be 5.7 pF. A cryostat with two different temperature regions has been developed for measuring the trap capacitance at low temperature. In this cryostat, Colpitts oscillator circuit is kept inside a MLI insulated box maintained at (290±1) K using heating element while the Trap temperature could be lowered to 96K by maintaining gas pressure at a controlled way as shown in Fig 3. Observed variation of 'F' with temperature is shown in Fig.4 indicating lowering of trap capacitance with temperature.

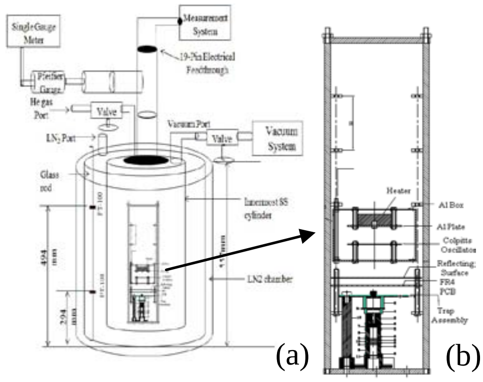

Fig3: (a) Cryo setup with two temperature regions (b) Holding Assembly

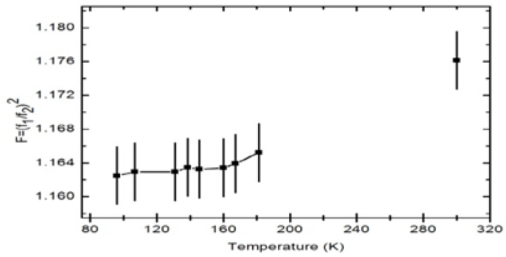

Fig.4. Variation of F at different temperatures

Results and discussion

Measured value of the capacitance of trap electrode assembly using Colpitts oscillator scheme is 5.7pF at room temperature and it decreases to 5.58pF at 96K. It is comparatively higher than the estimated value of ~2.6 pF based on trap geometry consideration and connected wires. The leakage of electric field at edge has not been considered while estimating capacitance of trap electrode assembly which is expected to be significant. Further simulation and improvisation of the scheme is in progress.

References

[1] D. J. Wineland and H. G. Dehmelt, J. Appl. Phys. **46**, 919 (1975)
[2] A.J. Slavin, Cryogenics **12**, 121 (1972)
[3] Agilent Impedance Measurement Handbook