High Precision 16K, 16Channel peak sensing CAMAC ADC

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Introduction

A high density, peak sensing, analog to digital converter (ADC) double width module with CAMAC back plane has been developed for nuclear physics experiments with a large number of detectors. This module has sixteen independent channels in plug-in daughter card mother board mode. The individual ADC daughter cards exhibiting excellent integral nonlinearity(≤±2 mV or ±0.02% full scale reading) and differential nonlinearity (≤±1%).

In this paper we describe the design and development of high precision (14 bit resolution) and high density (16 channels), with small dead time(<8 μs) ADC module. Commercially available modules such as the AD413 from EG&G ORTEC provides multiplexed, four-input, 8K ADC, with 6 μs conversion time per active input in a double width CAMAC module. The Philips model 7164 is a 12-bit ADC. This peak sensing ADC can be used in upcoming in National Array of Neutron Detectors (NAND) or Hybrid Recoil mass Analyzer (HYRA) at IUAC for multi element detector such as silicon strip detector with commercially available multichannel amplifier modules (mesytec, CAEN etc) with 34 pin FRC connector for input analog signal.

Block diagram & Functional details

The ADC module was designed using a successive approximation ADC with sliding scale correction technique, due to advantages of small conversion time with good resolution and linearity. We chose AD977A ADC chip from Analog Devices as it provides the smallest package and good linearity and simple two wire interface for data readouts. The value of differential nonlinearity (DNL) as per specification was ≤ ± 2 least significant bits(LSBs). The requirement for the application was ≤ ± 1%, and therefore a sliding scale DNL correction technique has been implemented. The individual ADCs for the sixteen channels are laid out on daughter cards that take care of all analog processing. The daughter cards plug into a mother-board through spring loaded gold plated contacts.

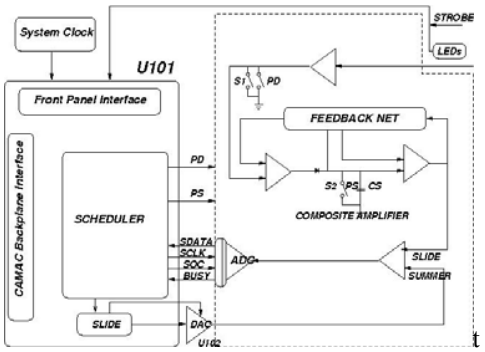

Fig. 1 ADC module internals

The central core of the module is the Spartan 3E Xilinx FPGA, (U101 of Fig.1) which is programmed in "VERILOG" to provide the backplane interface and necessary timing and control for analog and digital circuits. It also generates the necessary control signals for the ADCs. The entire operation is centered on the system clock. The data from the ADCs are simultaneously collected and stored in the FPGA through the two wire serial communication provided by the ADC chip.

The motherboard takes care of the two wire communication with each individual ADC, the CAMAC backplane interface and provides the triangular ramp for the sliding scale digital to analog converter(DAC) which is common to all the ADC daughter cards.

The daughter card consists of a serial ADC, sliding scale summer with gain matching, peak detection and peak stretch (PS), and input

voltage converters with differential inputs. The analog input is fed to a differential input front end so as to avoid the ground loop differences in different detectors and their corresponding shaping amplifiers.

These same daughter cards have been used earlier in the AD814 [3] (high precision 8 channel analog to digital converter) with clover detectors of Indian national gamma array(INGA) at IUAC.

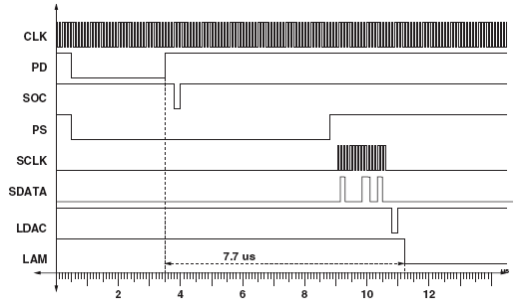

Fig. 2 Timing diagram initiated by a strobe

CAMAC back plane

The decoding of the CAMAC NAF commands is done by the CAMAC block of the FPGA, and it performs the required execution, returning the status and data as required. As configured at present the following functionality are implemented and can be directly accessed from the CAMAC backplane.

- Individual read of the sliding scale corrected ADC values.
- Clear all registers, busy, and LAM.
- Enable/disableLAM.

Performance and Specifications

The stringent requirements of the energy spectroscopy such as integral nonlinearity (INL) less than ±0.1% and DNL not more than ±1% were met. The alpha testing of the module exhibited better DNL and INL values. The beta testing was done with actual experimental setup in Detector lab at IUAC.

Table 1: Specifications

Function	***Value***
Resolution	14bit
No. of inputs	16
DNL	≤ ± 1%
INL	≤ ± 0.02%
Input range	0 -10V
Conversion gain	620 μV / channel
Dynamic range	0 – 16128channel
Dead time	7.7 μs for all channels

Conclusion

We have designed and fabricated a flexible, compact and economical ADC module suitable for nuclear physics experiments. Individual ADCs on daughter cards are based on a design without multiplexing, with a conversion time of 7.7 μs see Fig. 2. The possibility of design migration to any other backplane is also easy, which results from the plug-in ADC daughter cards model.

Acknowledgment

The authors would like to thank the Detector group, Inter University Accelerator Centre, New Delhi, and especially Akhil Jhingan for the help rendered in testing the module and suggesting appropriate improvements.

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