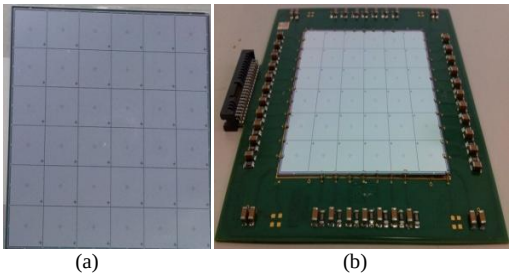
Characterization of 36 Pixel Silicon PAD Detectors

S. R. Narayan[1],* Shuaib A. Khan[1], J. Saini[1], P. Bhaskar[1], S. Mukhopadhyay[2], V.B. Chandratre[2] and Tapan K. Nayak[1]

[1]*Variable Energy Cyclotron Centre, Kolkata – 700064, INDIA*
[2]*Bhabha Atomic Research Centre, Mumbai - 400085, INDIA*
** email: rnarayan@vecc.gov.in*

Introduction

As silicon detectors offer good energy resolution and high reliability, these are ideally suited for tracking and calorimetric applications in nuclear and particle physics experiments [1]. The band gap of silicon is small enough to produce a good number of charge carriers per unit energy loss of the ionizing particles. Further, the high material density (2.33 g/cm^3) leads to a large energy loss per traversed length for ionizing particle (3.8 MeV/cm for a minimum ionizing particle) [2]. The semiconductor fabrication technology is now mature enough to produce low leakage and fast response detectors, as the mobility degradation is minimum due to doping. The planer semiconductor fabrication technology has been able to attain higher post processing carrier life time. The charge generated due to ionizing radiation can be rapidly and efficiently collected by applying suitable bias, within tens of nano-second. Therefore, these detectors can be used in high-rate count applications. The relatively lower sensitivity to magnetic field makes them very suitable for the high-energy physics experiments e.g. LHC experiments.



(a) (b)

Fig.1 (a) Silicon Pixel Array detector (PAD) with 6x6 pixels developed from a single wafer, (each pixel 1 cm^2) (b) PAD detector mounted on the PCB.

This paper discusses the initial characterization results of 6x6 silicon PAD (Pixel Array Detector) detectors, each pixel 1 cm^2, on 300 μm thick, and high resistivity wafer. The photograph of the detector is shown in Fig. 1. The objective of the development of the detector is to cater to high-energy physics experiment requirements. The detectors are designed by Electronics Division, BARC, fabricated at BEL, Bangalore and tested at VECC, Kolkata.

Detector Assembly and Setup

The detectors are fabricated on 6" wafers and are diced and then mounted on PCB. The PCB contains biasing elements along with provision to carry out static and dynamic tests. The highlight of the design is that it allows bringing connections of 36 pixels to the edge of the detector using single metal layer only. Individual pixels connection brought out at the edge of the detector are wire bonded to the PCB board on all the four sides, eleven each on two sides and seven each on the rest two sides. The four guard rings are bonded at each corner respectively. The signals from all the 36 pixels, from the anode of each pixel are taken by coupling capacitors and the biasing resistors located on the board. The common cathode is on the back side of the detector is connected to PCB with conductive epoxy. The 36-channel pixel detector after mounting on PCB is shown in Fig.1(b). During the testing, care has been taken to shield of the detector against ambient light and EMI. The static tests were done at BEL and VECC. Each of the pixels of the detectors was separately tested by keeping rest of the pixels grounded. The dynamic test for charge collection efficiency, noise was carried out by using beta sources setups as shown in Fig 2. A two-fold coincidence of the two scintillators is used as trigger for readout electronics. The pixel detector

PCB module is connected to the readout electronics modules via a backplane PCB. This backplane PCB is developed specifically to couple four detector modules and Front End Electronics (FEE) Board containing ASIC MANAS (Multiplexed Analog Signal Processor) [3]. The detector signals are connected to the FEE via a flexible Kapton cable. The two-fold coincidence from the scintillators is delayed by 1.2 µsec to match the peaking time of MANAS. The FEE boards are read through translator board (translates the LVTTL signal on FEE to the LVDS signal for long distance transmission and LVDS signal to back to LVTTL) by PCI-CFD data acquisition system [4].

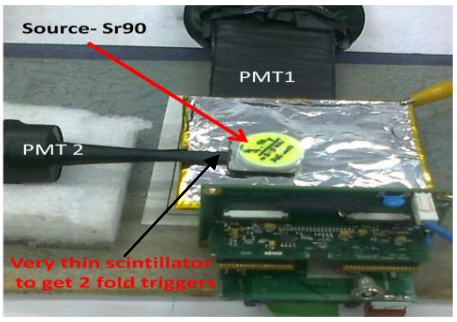


Fig. 2 Two-fold coincidence setup with detector coupled to MANAS

Results

In the static tests, the mean leakage current was less than 1.5 µA for total 36 pixels. Most of the pixels were found to be having leakage current less 40 nA. In C-V measurements as expected, the capacitance was found to be 40pF at full depletion voltage of ~ 45V.

In the dynamic test, optimum operating voltage of the detector was found to be 70 V using bias scan test where the RMS noise is minimum. Among 36 pixels these test are carried out with 32 pixels connected. Only one pixel showed higher than mean RMS noise as seen in Fig 3, the cause of pixel higher noise is investigated. In all these tests, guard rings were floating. The detector is also tested with Sr^{90}+Yt^{90} β-source; results shown in Fig. 4 are obtained after the pedestal subtraction with three sigma cut. Fig. 4(a) indicates that a single pixel is hit on the detector and Fig. 4(d) shows the hit position, predominantly of the single pixel on the detector. Sum ADC of all pixels and ADC for the selected channel are shown in Fig. 4(b) and 4(c).

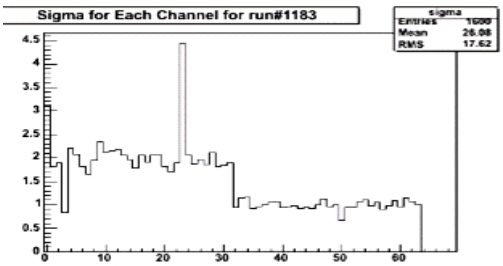


Fig. 3 RMS of individual Silicon pixel.

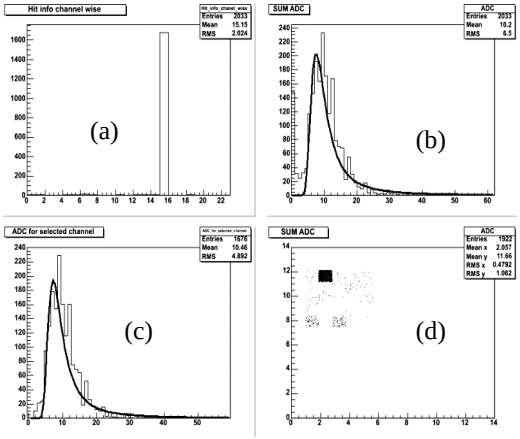


Fig. 4: Results from the PAD detector.

Acknowledgements

Authors like to thank Shri Y. P. Prabhakara Rao, Ms. Y. Rejeena Rani and Ms. Sapna Nayaka V. of BEL, Bangalore for their kind cooperation and for test done at BEL.

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