

Nuclear pulse data acquisition using a prototype FPGA based high speed data acquisition card

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Introduction

Digital signal processing concepts are nowadays being widely used in nuclear pulse data acquisition with most of these systems of late being developed using a Field Programmable Gate Array (FPGA) as a central processing unit. Functionality related to ADC interfacing, acquisition of data, subsequent signal processing and data transfer is implemented in hardware within the FPGA.

This paper briefly presents the features of an indigenously developed, FPGA based, two channel, analog input card with a maximum input sampling rate of 1 Giga samples per second (Gsp/s) per channel. The card has been used to digitize and acquire detector pulses. Salient design issues related to the associated hardware design and the application interface are also discussed.

Description

The card has been designed in a way that it can also work as a stand-alone system. The card can function as a platform for developing and evaluating different FPGA based hardware designs [1]. The features of the card are as follows:

- FPGA: Virtex-5 XC5VFX100T
- cPCI interface: 32 bit, 33MHz master interface with DMA transfer capability.
- Clock: On-board clock distribution for ADC and DAC.
- Rocket IO interface: Two SFP connectors.
- Memory: 2GB DDR2 – SDRAM; 256Mb flash memory
- Analog Input: Two channels using 12 bit, 1.0 GSPS ADC.

- Configuration: JTAG Mode; Using On-board Configuration PROM.

Analog input data is sampled, digitized and acquired within the FPGA. The digitized data is stored in First In First Out (FIFO) memory implemented within the FPGA. The data can be further processed and then transferred to the PC through the on-board PCI interface.

Salient Design Features

Pulse shape discrimination capability of a nTD Si detector in rare side injection mode has been studied using an indigenously developed 1 GHz sampling FPGA based digitizer [2]. Samples for this were acquired using a console based application developed in Visual C++ (VC++). Analog input from the pre amplifier was digitized and the samples were recorded for a time interval of 2 μ s starting from a fixed 500 ns (pre-trigger) before the arrival of an external trigger. The data was stored in the DDR2 RAM before transfer to the PC using the PCI based DMA mode. Recently, a new hardware design has been implemented within the FPGA. A major change relative to the previous design is that the design now is user configurable. The design has the following features:

1. Programmable pre-triggering mode: In this mode digitized samples before the trigger are also acquired. The number of samples to be acquired is user programmable.
2. Programmable acquisition of data: The number of samples stored in the FIFO starting from the pre-trigger is user programmable.
3. Internal trigger generation with Programmable threshold: If the digitized data is greater or less than (depending on the polarity of the pulse) the threshold, a

- trigger pulse is generated. The threshold is user programmable.
4. Programmable storage: Data from the FPGA based FIFOs is eventually transferred via PCI interface, using the DMA mode to the PC hard disk and stored in a Megabytes (MB).

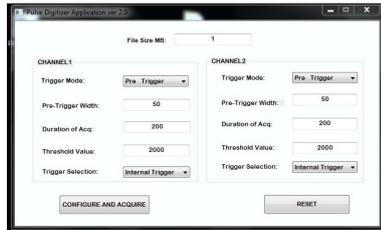


Fig. 1 GUI for data acquisition

The user programmable parameters viz. Pre-trigger width, number of samples stored in FIFO (Duration of Acq), threshold value, file size in MB are set through a windows based Graphical User Interface (GUI) written in VC++ (refer Fig. 1). These parameters are transferred to the FPGA through the PCI interface using the normal mode. These are stored in registers implemented within the FPGA.

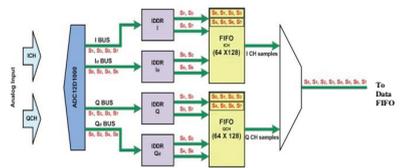


Fig. 2 Acquisition of data within FPGA

The hardware design consists of the following hardware entities:

1. Configuration and calibration of external clock synthesizer.
2. Configuration of ADC.
3. Data acquisition of digital samples within the FPGA.
4. Sample rearrangement and concatenation for further processing. This is done using a FIFO implemented within the FPGA.
5. Transferring of data to PC via PCI FIFO.

An output reference clock of 250 MHz is provided by the ADC to the FPGA for acquiring

data. The data coming from the ADC is double data rate (DDR) on all the four buses. Hence the effective data rate is $250 \times 2 = 500$ MHz on each data bus (refer to Fig. 2 and Fig. 3 for more details).

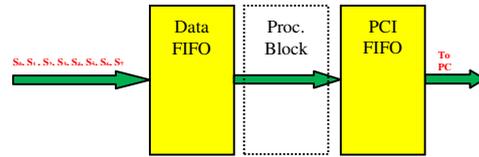


Fig. 3 Acquisition of data within FPGA

ADC provides the reference clock to the FPGA for each channel (I and Q) and the samples are latched on every rising edge of the clock pulse. Initially DDR data is sent by the ADC which is converted to Single Data Rate (SDR) data by using the IDDR primitive available within the FPGA. Hardware within the FPGA is designed in a way that if the acquired data is to be further processed, then the processing algorithms can be implemented after the Data FIFO and before the PCI FIFO. Thus data is first read from the Data FIFO, processed and then written into the PCI FIFO for transfer to the PC.

Conclusion

A FPGA based, two channel, analog input card with a maximum input sampling rate of 1 Giga samples per second (Gsp/s) per channel has been indigenously developed and is being utilized for pulse data acquisition. Currently, two channels can be successfully digitized simultaneously at 1 Gsp/s. Each channel is able to sustain a pulse rate of 1 KHz.

References

- [1] A FPGA based high speed data acquisition card. J.A. Gore et al, proceedings of PCaPAC'2012, Kokata, India, pp 271-273
- [2] Particle identification using pulse shape discrimination in a nTD silicon detector with a 1 GHz sampling digitizer. K. Mahata, et al. International Symposium on Nuclear Physics, 2013, Mumbai.