Readout Boards for Silicon Detectors

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Introduction

With ever increasing demands for greater miniaturization and the use of sophisticated circuitry in nuclear and particle physics experiments, the need for improved design of Printed Circuit Boards (PCBs) is becoming more important day by day. Interconnecting traces, parasitic components, grounding schemes and decoupling makes the design of the layout of PCBs as demanding as the design of the complex electrical circuit. An astute design of the readout boards is important in the success of the overall performance of the final system.

These obligations are more stringent, while designing the boards for silicon detectors. PCB effects that are harmful to precision circuit performance includes leakage resistances, which is one of the most important parameter in silicon detectors, IR voltage drops in trace foils, vias, and ground planes, the influence of stray capacitance, and dielectric absorption. In addition, the tendency of PCBs to absorb atmospheric moisture means that changes in humidity often cause the contributions of some parasitic effects to vary every-day.

Taking into account the contention of leakage currents, space constraints and integration issues of the detector and readout assembly; development of readout PCB boards for silicon detectors to be used in Electromagnetic Calorimeter at LHC experiment are presented in this paper.

Design issues

Each experiment uses a unique approach, in which preference of the designers and the industry support plays a major decisive role. The proposed Electromagnetic Calorimeter (EMC) in the forward rapidity region of ALICE experiment at CERN [1], will be a novel compact, sampling type silicon-tungsten sandwich design, requires highly granular layers of detectors consisting of $1mm^2$ as well as $1cm^2$ silicon pad detectors. The interleaving spaces between the two tungsten sheets available for the readout is only 3 mm, it has to be minimum for the containment of the electromagnetic shower.

Considering the stringent design requirements of the experiment, the PCB design of silicon detectors as well as for its readout boards itself poses a challenging job, since layer to layer dead space and space between each silicon element has to minimum. The PCB having 300 µm thick silicon pad detector along with biasing components should be the only material between the interleaving spaces of the tungsten sheets. To meet this challenge, a 0.8 mm thick, FR4 grade glass epoxy multilayer PCB is designed, with 25 silicon PAD detector, each $1cm^2$, on 10 cm x 10 cm PCB, preserving the element to element compactness of the detector as shown in Fig. 1.

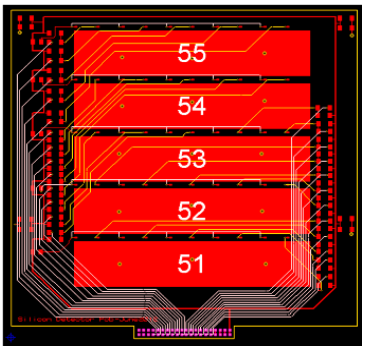

Figure 1. The Detector PCB layout, each row for five $1cm^2$ silicon PAD detector.

Signals from this detector PCB is integrated with the front-end electronics (FEE) board for the readout of the detector. Separate readout boards were used for reading with different

ASIC's. For this purpose a four layer PCB, was developed, for reading with ANUSANSKAR [2] and a six layer PCB for reading with MANAS which was designed earlier (used for silicon detectors with slight modifications), shown in Fig. 2 (b) and Fig. 2 (c). These detector PCBs are mounted on backplane PCB from the bottom side while the FEE boards have been mounted from the top side. Two different back plane PCBs have been designed in such a way that we can mount either two MANAS ASIC or 4 ANUSANSKAR ASIC FEE boards to read all 100, 1cmx1cm silicon pads silicon pads from four layer of detector PCBs as shown in Fig. 3. This figure shows the test beam arrangements in the PS beam line at CERN.

(a) (b) (c)

Figure 2. (a) Two kinds of backplane PCBs, (b) FEE board for ASIC ANUSANSKAR, and (c) FEE board for ASIC MANAS.

All the electronic components used on detector PCB and readout boards are surface mount type (0603 size), which have almost zero interlead capacitance. Properly designed multilayer PCBs also reduce EMI emissions and increase immunity to RF fields, by a factor of 10 or more, compared to double-sided boards [3]. For the development of all the above mentioned readout boards and detector PCBs, high glass transition temperature (Tg) Tg135/170 material is used, so the material will typically not transit beyond the Tg in assembly and soldering processes [4]. With a surface finish of gold and no green mask protective coating. It was observed in the lab that this configuration reduces the leakage current.

Strict design specifications of track to track spacing, track to pad spacing, pad to pad spacing and trace width of 6 mil (1 mil = 0.0254 mm), plated through hole for the outer diameter is 20 mil and for the inner diameter is 10/12 mil for each board, is strictly followed. These readout boards have been fabricated. Silicon detectors were mounted and readout by using these boards. They are found to work well in test beam experiments at CERN.

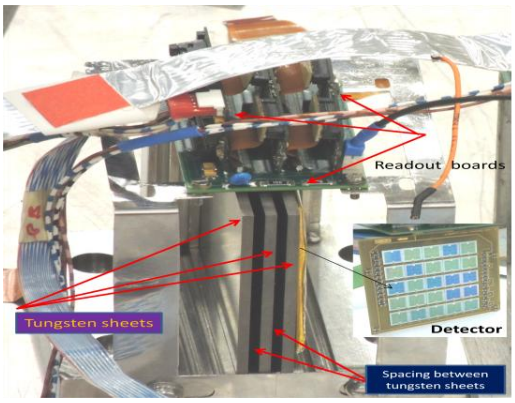

Figure 3. Test setup arrangement showing the integration of prototype tungsten-silicon detector and its readout.

Acknowledgements

Authors would like to thank Shri Y. P. Prabhakara Rao, Ms. Y. Rejeena Rani and Ms.Sapna Nayaka V. of BEL, Bangalore for their kind cooperation and detector fabrication done at BEL.

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