

## FPGA Emulator of GBTx for Muon Chamber (MUCH) in CBM Experiment

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### Introduction

A Gas Electron Multiplier (GEM) based detector system is being developed at VECC, Kolkata for use as muon tracker in the Compressed Baryonic Matter (CBM) experiment at the upcoming FAIR facility at Germany [1]. Muon Chamber (MUCH) is used to detect low momentum muons in an environment of high particle densities. Detecting these set of particles require fast and radiation-hard detector systems, which are positioned in dense arrangements and to be readout by radiation hard front-end electronics (FEE). To read such high data rate, CBM requires precise time synchronization, compact hardware, radiation tolerance, self-triggered front-end electronics. For efficient data aggregation from these FEE's, GBTx (developed by CERN) is planned to be used as a bridge to the Data Acquisition (DAQ) system. As this ASIC is radiation hard, we are restricted to bring these GBTx ASICs to India. This article focuses on the implementation of this GBTx into a FPGA (Field Programmable Gate Array) board for CBM- MUCH detector.

### CBM Network and DAQ Structure

The simplified read out architecture of MUCH to be used in CBM experiment is shown in Fig.1. In Muon Chamber fast and highly granulated GEM detector is to be used. The MUCH-XYTER a radiation hard ASIC used for signal detection from MUCH in the CBM environment. The self-triggered ASIC provides both timing and energy information for each incoming signal in its channel. MUCH-XYTER is connected to the Gigabit Transceiver (GBTx) in the back end through SPI-like e-links. The GBTx is a radiation tolerant chip that can be used to implement multipurpose high speed bidirectional optical links for high-energy

physics experiments [2]. It is connected with Data Processing Board (DPB) through optical fiber. DPB will be placed outside the irradiated area and more complex electronic systems like commercial-off-the-shelf (COTS) FPGA and faster optical links can be used in this layer [3]. DPB will be connected to the First Level Event Selector interface Board (FLIB) through 10 Gbps optical link. Finally FLIB will transmit data to the computer using PCIe. As a Part of the development of DAQ here we have concentrated in the implementation of GBTx in FPGA.

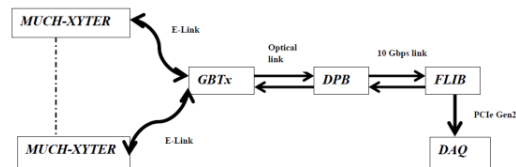


Fig. 1 DAQ Chain

### Gigabit Transceiver (GBTx)

The simplified block diagram of GBTx is shown in Figure 2. Here pattern generator and pattern checkers are used for testing purpose. But when it is connected with the read out chain they will replace with fifo which will store data from MUCH-XYTER. Scrambler is mainly used for accurate timing recovery in the receiver side. It also reduces inter carrier interference.

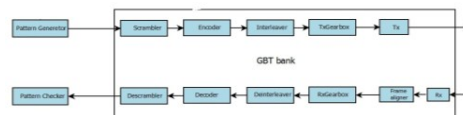


Fig. 2 Internal Architecture of GBTx

In the encoder block single error correcting (15, 11) Reed-solomon encoding is used. Input data to the scrambler is 84 bit. When data will enter into the encoder block it will append with

four bit header. This channel coding can correct maximum eight symbols consecutively.

Output of the encoder is 120 bit data. Interleaving is the reordering of data that is to be transmitted so that consecutive bytes of data are distributed over a larger sequence of data to reduce the effect of burst errors. Data width after interleaver block remains 120 bit. But this 120 bit data cannot be send at a time so a Gearbox is used. It will divide 120 bit data into three 40 bit words and send it to Multigigabit Transceiver (MGT).GBTx frame sent to the transmitter consists of four bit header, four bit data for slow control, 80 bit raw data, and 32 bit data for forward error correction. The GBT frame is shown in figure 3.



Fig. 3 GBTx frame format

Receiver side of GBTx performs just opposite jobs like deinterleaving, decoding and descrambling. Only the framealigner block in receiver side is not present in transmitter side. It consists of:-Pattern Search block, Bitflip Counter, Right Shifter, Write Address generator. Pattern search block continuously check whether proper four bit header is received or not. Until the proper header is received bitflip counter continuously change its value. After receiving correct header write address generator will generate address in the RAM where 40 bit data will be written.

### Implementation on FPGA

For implementation of the GBTx code, we have used xilinx KC705 board. Here two clocks are used:- FPGA fabric clock whose frequency is 156.25 MHz and MGT reference clock whose frequency is 120 MHz. FPGA fabric clock is generated internally from Si570 3.3V LVDS I<sup>2</sup>C Programmable Oscillator. MGT reference clock has to be very low jitter clock. In the figure 4 clock is given form external pulse generator. Output of the pulse generator is LVTTTL and MGT reference clock input is LVDS. For this reason one translator board is used between pulse

generator and FPGA board. Result we obtained is shown in Fig. 5.

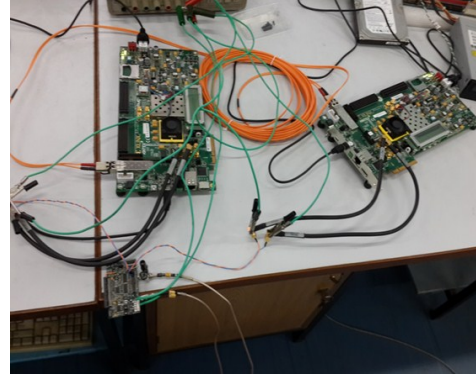


Fig. 4 Setup in VECC using for testing GBTx

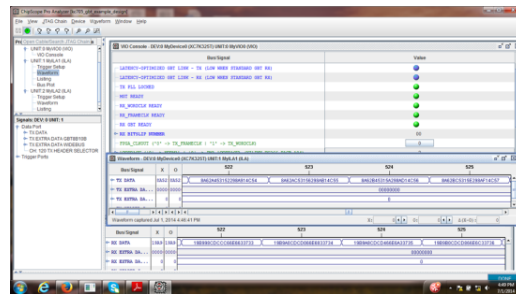


Fig.5 Testing of GBTx using Chipscope

From the figure 5 it is observed that MGT transceiver is ready and working properly. We have received the same data that we have transmitted.

### References

- [1] CBM Technical Design Report 2013(TDR).
- [2] P.Moreira, J.Christiansen and K.Wyllie,," The GBTx Link Interface Asic," v1.7 Draft, Oct.2011.
- [3] K.Kasinski, W.Zabolotny and R.Szczygiel, "Interface and protocol development for STS read-out ASIC in the CBM experiment at FAIR," in Proc. Photonics Applications in Astronomy, Communications, Industry, and High-Energy Physics Experiments, 2014.