Prototype VME & CAMAC form factor Timestamping module development for Nuclear Physics Experiment

Ram Kumar Paul*, Partha Dhara, Pintu Maity, Pranab Singha Roy and Amitava Roy

Data Acquisition & Computer Control Division, Variable Energy Cyclotron Centre, Kolkata- 700064, INDIA
** email: rampaul@vecc.gov.in*

Introduction

The modern nuclear physics experiments employ large detector arrays for measurement of different radiations, like charge particle, Gamma, Neutron etc. Heterogeneous detector systems may have different response time and different front end processing. The trigger rate of the individual detector system, as well as the width of the acquisition window may vary accordingly. It may not be possible to generate a common GATE signal to acquire correlated events, without introducing significant dead time. It is proposed to run multiple DAQ (Data Acquisition System) independently on its own trigger and mark the data with high-resolution timestamps. Timestamp may be the absolute time or a local counter value. The offline event builder generates the global correlated events by matching the timestamp values.

Timestamping Scheme and parameter requirements

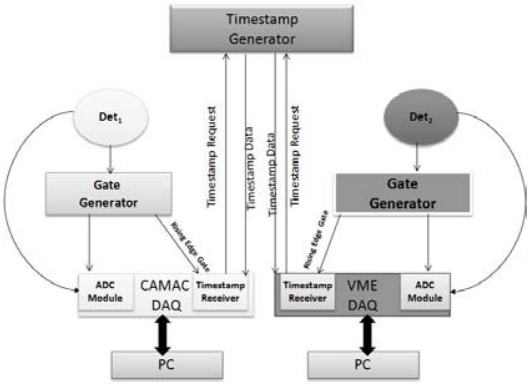

Fig.1 Timestamping Scheme

Timestamp has been generated in an independent *Generator* module and each DAQ has a *Receiver* module. The *Generator* module delivers the current timestamp value on request from the *Receiver* module. Each DAQ works with its own trigger rate and on every trigger it request for corresponding timestamp. Events are tagged with the timestamp value and stored in a list file. The offline event builder merges the timestamped events within a small time window to build the global correlated event. The typical GATE width for nuclear spectroscopic experiments varies between 1µs to 6µs, ADC conversion time is of the order of 6 µs and 1 µs needed for tagging and storing data in FIFO. Therefore, the timestamp data from the Timestamp *Generator* has to reach *Receiver* module within 8µs.

Timestamp *Generator* is designed for 10ns timing resolution and suitable for spectroscopic application.

DAQ Software Modification

The DAQ Software has been updated to accommodate timestamp data [1, 2]. Current solution reads 48-bit timestamp from VME & CAMAC Timestamp Receiver module. F# based routine has been developed to merge timestamp data for offline analysis.

Timestamp Generator module

In this module, a 48-bit free running counter is operated at 100MHz clock. The timing resolution is 10ns and it can run continuously 32 days before roll over. The data is latched at the rising edge of the clock signal, avoiding bit racing error, without stopping counter. On request from *Receiver* module, this module latched the counter value at that instant in a 48-bit register. For error free communication, it generates the 16 bit CRC corresponding to latched data using CRC-16-CCITT polynomial, $X^{16}+X^{12}+X^{5}+1$.

A two-wire serial communication protocol has been used for *Generator* and *Receiver* communication. The serial data frame consists of one Start bit followed by 48 bit timestamp information and 16 bit CRC value. This

Generator module has also been tested for deliberation of four independent requests from four *Receiver* modules.

Timestamp Receiver module

For every CAMAC and VME crate, one timestamp receiver module is placed within the crate. The module sends a timestamp REQUEST pulse to *Generator* on the rising edge of the GATE signal. The receiver modules check the received data frame by computing the CRC of the received frame. The valid data gives zero CRC output and stored in a register. The erroneous data produces non-zero CRC and are tagged as BAD timestamp. The timestamp data are then read through CAMAC or VME DAQ along with the event data.

❖ CAMAC form factor based Timestamp Receiver module

CAMAC Receiver module has been developed using our in house developed Spartan-2 FPGA board. This module has four input ports at front side, one for input gate trigger, one for REQUEST to *Generator*, one for serial data input from *Generator* and one for busy output for synchronization module. The back end of the module is CAMAC form factor compatible.

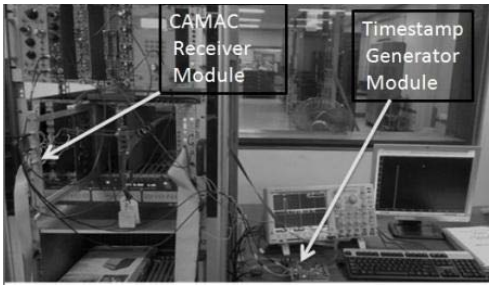

Fig. 2 Timestamping Experiment set up for CAMAC Data Acquisition System

❖ VME form factor based Timestamp Receiver module

We have used CAEN V1495, General Purpose VME Board to develop VME form factor based timestamp receiver module. This board can be directly customized by the User, and it houses two FPGAs. The first one is the FPGA "Bridge", used for the VME interface and for the connection between the VME and the second FPGA (FPGA "User") through a proprietary local bus. We have developed the VHDL code to program user FPGA for timestamp receiver module. The code is programmed to the user FPGA "on the fly" via VME. The 32 bit VME FIFO BLT read is used to read the timestamp data.

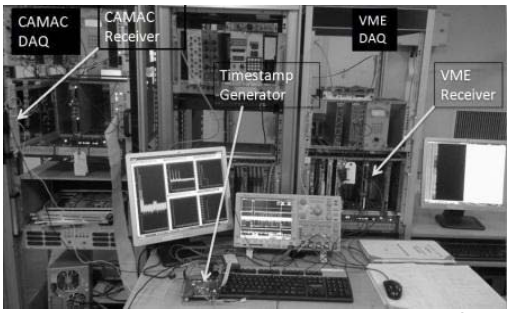

Fig. 3 Timestamping Experiment set up for CAMAC & VME Data Acquisition System

Experimental Results and Discussions

The Generator Receiver communication has been tested with two 1 meter long coaxial cables and achieved communication data rate up to 100MB/s. With this data rate, the timestamp data arrive at *Receiver* module within 5.8µs from *Generator* module.

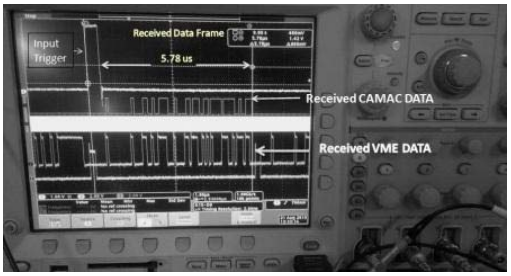

Fig. 4 CAMAC & VME Data Frame

Automata are tested up to 10 KHz of random and up to 100 KHz of periodic trigger inputs. The accuracy and the consistency of the timestamps have been verified for different input trigger rates, using the DAQ software.

References

[1] P. Dhara et al., "Multi-threaded object-oriented VME data acquisition system on Linux", DAE-BRNS Symposium on Nuclear Physics, Vol. 46B, p. 530-531 (2003).

[2] P. Dhara et al., "Integration of CAMAC system in VME based DAQ Software", DAE-BRNS Symposium on Nuclear Physics, Vol 50, p. 454 (2005).