ANUSPARSH-II frontend ASIC for avalanche mode of RPC detector using regulated cascode trans-impedance amplifier

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Introduction

This paper presents the design aspects and test results of ANUSPARSH-II frontend ASIC, intended for readout of INO-ICAL Resistive Plate Chamber (RPC) detector. This ASIC is designed and fabricated in 0.35 um CMOS process as an eight-channel, high speed, low power amplifier-discriminator frontend solution for avalanche mode of operation of INO-ICAL RPC detector. In this ASIC, a regulated cascode (RGC) trans-impedance pre-amplifier is used for the first time as frontend of RPC detector exhibiting input impedance matched with the characteristic impedance of RPC pick-up strips.

The ANUSPARSH-II ASIC is tested with 1m x 1m RPC detector at TIFR and BARC, meeting its designed specifications. As the input impedance of ANUSPARSH-II ASIC is very low, it is also interfaced successfully with commercial Multi-Photon Pixel Counter (MPPC) and indigenously designed high gain photo-diode array structures, maintaining the signal bandwidth.

ANUSPARSH-II ASIC design

The ANUSPARSH ASIC is designed to meet the INO-ICAL RPC readout requirements of (1) total channel gain of ~ 6 mV/uA for avalanche mode of detector operation, (2) amplifier rise time of ~ 1.2 ns, (3) input impedance matched to RPC pick-up strip impedance, (4) identical performance for single ended inputs of both the polarities obtained from X & Y pickup strips, (5) availability of amplifier output for detector signal profile analysis and (6) low power consumption. The first version of ANUSPARSH ASIC comprised eight identical frontend channels consisting of regulated cascode trans-impedance amplifier, two-stages of differential amplifier, fast leading edge discriminator with LVDS output and multiplexed analog ~50 Ω cable driver buffer [1]. In the RGC architecture the common gate input impedance ($1/g_{m1}$) is reduced by loop gain (g_{m2}*R2) of a local feedback loop enabling required impedance matching with the characteristic impedance of RPC pickup strip over wide frequency range as shown in Fig 1. The RGC is generally used in optical communication and is used for the first time as RPC detector FE, implemented in ASIC.

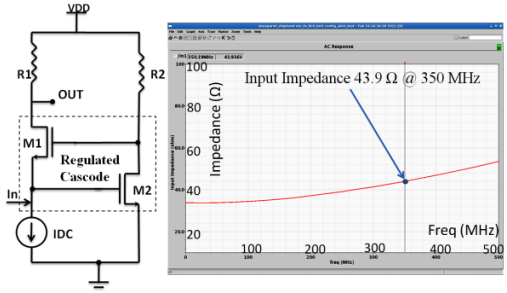

Fig. 1 Simplified regulated cascode amplifier and simulated input impedance vs. frequency

The second version of ANUSPARSH ASIC is built around the same core architecture as of the first version with additional common mode feedback and dynamic offset compensation circuits [2] for DC bias and gain stability across readout channels. In this version differential inputs are provided with the other input being used as local RF ground thereby enhancing the noise performance. Using this scheme identical polarity of amplifier output is obtained at the discriminator input for both X and Y complimentary input signals, resulting in common threshold adjustments in X & Y-side FE boards. Further, in ANUSPARSH-II ASIC, a

dynamically biased ~50 Ω cable driver buffer [3] is incorporated providing reduction in the buffer power consumption by a factor of four.

A two-chip amplifier and discriminator frontend solution for INO-ICAL RPC detector is also designed in 0.35 um SiGe BiCMOS process and is under field trial.

Test Results:

The ANUSPARSH-II ASIC is tested with 1m x 1m RPC detector at TIFR for detector efficiency, stable noise rate and timing spectrum.

Table 1: Tested specs of ANUSPARSH-II ASIC

Total channel gain	~ 6 mV/uA
Amplifier rise time	~ 1.2 ns
LVDS common mode range	0.8V to 1.6V
Timing Accuracy	~ 72 ps
Power Consumption per Channel	~ 45 mW @ 3.3 V supply
LVDS output rise time	~700 ps

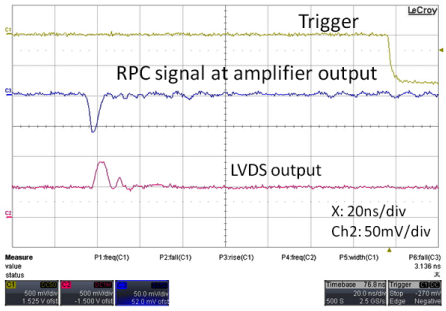

Fig. 2 Amplifier & discriminator LVDS output

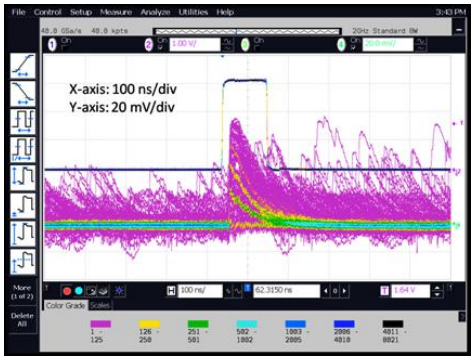

Fig. 3 Results with MPPC detector

These tests showed stable noise rates, timing spectrum sigma of ~1.6 ns and single strip efficiency of ~ 75% with respect to a trigger from two-fold coincidence of telescopic scintillators of width less than the pick-up strip width. The test results are shown in Fig 1 and Fig 2. The ANUSPARSH-II ASIC is also characterized at BARC on 1m x 1m RPC detector [4]. Further, the ANUSPARSH-II ASIC is also successfully interfaced to the commercial MPPC detector and indigenously designed high gain photo-diode array structures exhibiting single and multi-photon peaks, as shown in Fig. 3 and Fig. 4 respectively.

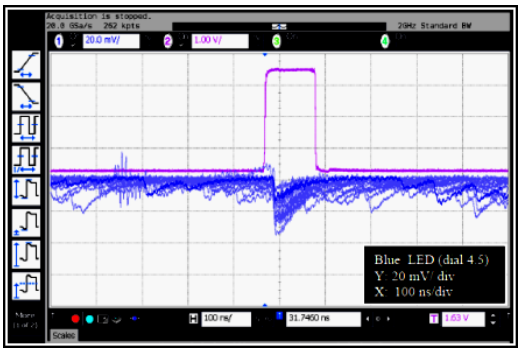

Fig. 4 Single and multi-photon peaks with in-house high gain photo sensors

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