Portable Digital Pulse processing for γ ray spectroscopy

Madhusudan Dey[1],* Santu Ghosh[1], Rintu Bhaskar[2],†
Aritra Ray[2], Sounava Chakraborty[2], and Rajni Gupta[3]
[1] *Variable Energy Cyclotron Centre, Kolkata-700064, INDIA*
[2] *Jadavpur University, Kolkata-700032, INDIA and*
[3] *Maulana Abul Kalam Azad University of Technology, Kolkata-700064, INDIA*

Introduction

Digital pulse processing of nuclear pulses from different types of detectors needs digital algorithms to extract meaningful information such as energy, timing etc. from the processed signals. A host of analogue modules that perform the actions of constant fraction discriminator(CFD), baseline restoration and peak searching are eliminated by the uses of digital modules. A Data Acquisition firmware with ethernet connectivity is implemented using FPGA for spectroscopic measurement for our in house nuclear and particle physics experiments.

Hardware

The digital pulse processing system contains FPGA board and an ADC board@125 MSPS. A block diagram of the processing modules of a single channel digital pulse processor is shown in Fig. 1 [1] where input range of ADC is 0 - 1000 mV.

Trapezoidal Filter

The difference equations of the algorithm used in this application are shown below. The filter takes the digitized nuclear pulse x(n) as an input and converts it into a trapezoidal pulse g(n) by using Eq.1 to Eq.4 [2]. W is the factor having relationship with decay time of the pulse and k and l are sequence numbers.

$$y^{kl}(n) = x(n) - x(n-k) - x(n-l) + x(n-k-l). \quad (1)$$

$$e(n) = e(n-1) + y^{kl}(n), n \geqslant 0. \quad (2)$$

$$f(n) = e(n) + W y^{kl}(n). \quad (3)$$

$$g(n) = g(n-1) + f(n), n \geqslant 0. \quad (4)$$

CFD

As shown in Eq.5 input and output of CFD are x(n) and q(n) respectively, Const is usually 0.5 and d is delay of the order of 3 [3].

$$q(n) = Const * x(n) - x(n-d). \quad (5)$$

Peak Searching

Peak searching of the nuclear pulse is done using trigger signal. It starts at i^{th} trigger and it remains high for pre-calculated time. Maximum value of the pulse is obtained when trigger is high between i^{th} and $(i+1)^{th}$ trigger.

$$\begin{aligned} Peak_i = max_i(x_0, x_1, ..x_n), where \\ trig_i < trig_{searching} < trig_{i+1}. \end{aligned} \quad (6)$$

Firmware Architecture

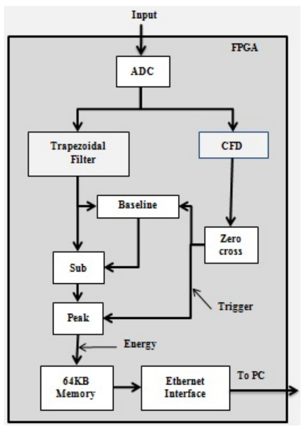

FIG. 1: Firmware block diagram.

*Electronic address: msdey@vecc.gov.in
†Electronic address: rintu.bhaskar.10@gmail.com

The CFD, Trapezoidal Algorithmic filter and processing and computations within FPGA are implemented in fixed point format. The length of the format, its precision, scaling and resizing are adjusted to suit the accuracy of the pipelined computations [4],[5].

Experimental setup

This pulse processing instrument has been tested using Co^{60} and Cs^{137} sources having energy of 1173KeV, 1332KeV and 662KeV using HPGe detector. The calibration was found linear within the energy range of 511KeV to 2500KeV.

Experimental results

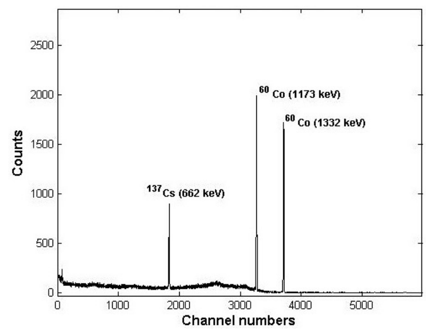

FIG. 2: Spectrum of different γ energy.

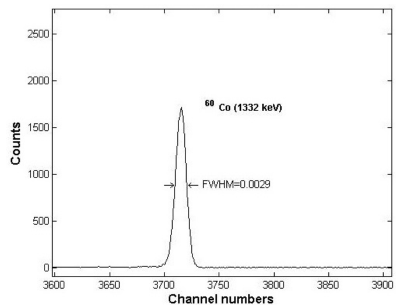

FIG. 3: Blow up peak of Co^{60} 1332 KeV energy.

The test result shown in Fig. 2 is the 1D spectrum of the sources used in this experiment. The channel spread is of the order of 11 in 8k channels and the electronic resolution is of the order of 0.08% with FWHM 0.0029 as in Fig. 3.

Conclusion

Developed system can be used connecting directly to a preamplifier of HPGe detector provided that the pulse shape is exponential and the decay time is long enough ($\approx 100\mu$s). It can also be configured for lower decay time from 5μs onwards. Suitable exploration was also done for inorganic scintillators detector and found reasonable to use.

KeyWords: FPGA - Field Programmable Gate Array, MSPS - Mega Samples Per Second, FWHM - Full width half maximum.

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