DAQ system for testing RPC front-end electronics of the INO experiment

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Introduction

The Resistive Plate Chamber (RPC) is the active detector element in the INO experiment. The in-house developed ANUSPARSH–III ASICs [1] are being used as front-end electronics of the detector. The 2 m X 2 m RPC being used has 64-readout channels on X-side and 64-readout channels on Y-side. In order to test and validate the FE along with the RPC, a 64-channel DAQ system has been designed and developed. The detector parameters to be measured are noise rate, efficiency, hit pattern-register and time resolution. The salient features of the DAQ system are: 64-channel LVDS receiver in FPGA, FPGA based parameter calculations and a micro controller for acquiring the processed data from FPGAs and sent through Ethernet and USB interfaces.

The DAQ system consists of following parts: Two FPGAs each receiving 32 LVDS channels, FPGA firm-ware, micro controller firm-ware, Ethernet interface, embedded web-server hosting data analysis software, USB interface, and Lab-windows based data analysis software. The DAQ system has been tested at TIFR with 1 m X 1 m RPC.

FPGA Firm-ware: measurement of parameters and data communications

The DAQ system has two FPGAs; each FPGA receives 32 LVDS channels from FE. The FPGA firm-ware consists of following parts: LVDS receivers, parameter calculation, communication between FPGAs, FIFO and readout interface with micro controller. The LVDS line receivers have been instantiated in the FPGA to directly receive the LVDS signals.

The firm-ware has been designed and developed in Verilog HDL to measure the following parameters. Noise rate, efficiency and hit-pattern register are the important parameters to assess the long-term stability, dark current, particle tracking ability and directionality of the detector [2]. To measure noise rate and efficiency, a time interval of one second has been derived inside the FPGA from system clock of 50 MHz. The pulses from each channel which are falling in the one second interval are counted to measure the rate in counts per second (CPS). One channel among the 64–channels can be selected for efficiency with help of on-board selection switch. The ratio between the RPC pulse count in coincidence with the trigger and trigger count gives the efficiency. In order to cater to trigger latency a pulse stretch logic has been designed. The hit pattern register is designed to know the position of the particle interaction. In this the status of all the stretched pulses has been latched on trigger. In order to find the time resolution a TDC has been designed and developed in FPGA.

The 32 channel data measured in FPGA1 has been transferred to FPGA2 and further all the 64 channels are interfaced with FIFO. Both serial (SPI) and parallel interfaces have been designed and developed to interface the FPGA FIFO with the micro controller to transfer the parameter data.

Micro controller Firm-ware: Acquisition of parameters data, Ethernet and USB interface

The micro controller receives the data from FPGA and stores in corresponding parameter arrays. The micro controller used is based on ARM Cortex–M3; it has internal Media Access Controller (MAC) and Physical (PHY) layers for Ethernet interface. It also has an internal USB

controller. The data is sent to the PC via Ethernet or USB interfaces.

The Ethernet stack consists of PHY, MAC, LwIP Protocol and an embedded web server has been configured. The web server based on LwIP is designed to host HTML and JAVA based web pages. These web pages consist of data analysis software for online displaying of 64-channel noise rates, efficiency and hit pattern. The webpage also consist the options for storage of data for offline analysis.

The USB is configured as Communication Device Class (CDC) to send the micro controller data to PC. On the PC side a serial emulator driver is installed to read the data on PC COM port. The data analysis software designed in lab-windows read the data from COM port to display and store the parameters.

Experimental Setup and Test results:

The DAQ system has been tested with 1 m X 1 m RPC and ANUSPARSH-III ASIC FE electronics at TIFR. The experimental setup is shown in Fig. 1.

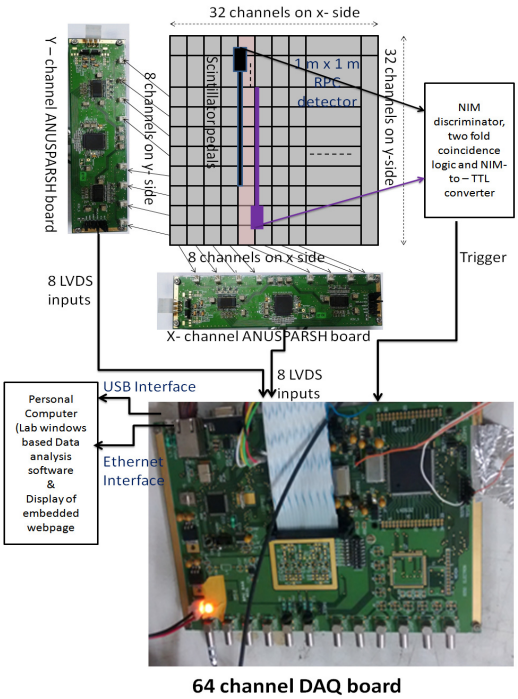

Fig. 1 Experimental setup showing the 64 channel DAQ system

The LVDS outputs from the 8-channel X-side FE board and 8-channel Y-side FE board are connected to the DAQ system. The pulse rates from the RPC strips have become stable after the LVDS cable is properly terminated on the board.

To measure the RPC strip efficiency, two scintilator pedals covering single strip have been placed one on top and another at bottom of the RPC. A trigger pulse from the coincidence of two scintillator pedals has been derived. The ratio between the RPC pulse count in coincidence with the trigger and trigger count gives the efficiency.

Measurements for noise rate and efficiency have been taken by varying the threshold voltage of the FE and the results are listed in the Table 1. The threshold voltage has been varied from 60 mV to 25 mV. Fig. 2 shows the plot for noise rates of the RPC in CPS.

Table 1: Rate & efficiency vs. threshold voltage

Threshold Voltage	Noise rate in CPS	Efficiency
60 mV	~ 20 CPS	86.6%
40 mV	~ 30 CPS	89%
30 mV	~ 40 CPS	91.5%

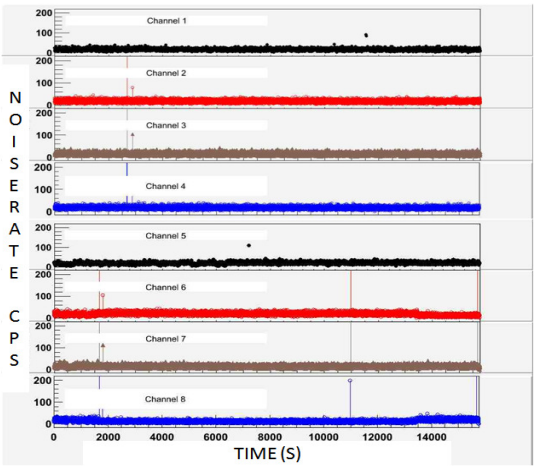

Fig. 2 X-side noise rate plots at 60 mV threshold

References

[1] Proceedings of VCASAN, 258, Springer India (2013), 71.
[2] Nuclear Instrumentation Methods 187, (1981), 377.