GBT link testing and performance measurement on Altera Stratix-V FPGA

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Introduction

The particle physics experiments at CERN-LHC are aiming to collect data at high luminosity to exploit the full physics potential and improve the statistical accuracy of the measurements [1]. However, it will also impose more stringent requirements on the performance of the data acquisition systems as well as on their radiation tolerant characteristics. In particular, the data transmission links will have to be upgraded to wider bandwidths in order to cope with the larger amounts of physics data being produced by the detectors. So a joint effort is made by the CERN team to build radiation tolerant high speed data communication architecture [2]. A Gigabit Transceiver (GBT) architecture was developed under this perspective. The GBT is a radiation tolerant chip that can be used to implement multipurpose 4.8 Gbps bidirectional optical links in hostile radiation environment for particle physics experiments as shown in fig 1.

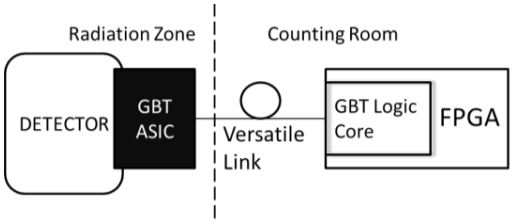

Fig. 1 Link architecture with GBT chipset and the versatile link

A GBT chipset is used for packaging of detector data and transmitting it in GBT standard. While the point to point optical link connecting the GBT ASIC with the Field Programmable Gate Array (FPGA) is termed as Versatile Link. It gives the specification of the optical fibre, Small Form Factor Pluggable (SFP) connector and transceiver type to be used during interfacing. A firmware developed by CERN known as GBT FPGA Logic Core can be loaded in the FPGA reconfigurable electronics hardware. It makes the FPGA to behave as GBT ASIC for receiving the GBT datagram. The aim of such architecture is to allow a single bidirectional link to be used simultaneously for data readout, trigger data, timing control distribution, experiment slow control and monitoring.

GBT link

The GBT Link is the actual channel of the link. It is composed by a GBT transmitter (that scrambles and encodes the transmitted parallel data), a Multi-Gigabit Transceiver (MGT) (that serializes, transmits, receives and de-serializes the data) and a GBT receiver (that aligns, decodes and descrambles the incoming data stream). It takes data from the user application layer in parallel data format and wraps it in GBT specified standard to transmit in a serial optical link. The GBT link provides the users with two modes of operation: standard and latency optimized mode of operation. Each link also supports two types of coding scheme, namely GBT Frame and Widebus coding. The data bus available to the user application layer depends upon coding used and the packet header appended.

GBT link testing and performance measurement

In standard mode of operation, the data transfer has an uncertainty of +/- one clock cycle in the transfer time. In latency optimized mode, data transfer features register based Clock Domain Crossing (CDC) for deterministic latency. Register based CDC requires calibration, to guaranty a stable behavior over a comfortable operating temperature range. For the GBT link test in Altera Stratix-V it was observed that the word clock (clock at which the data is sent out of

the link) is not locked at proper phase and sampling the frame data (data received at the link) at incorrect point as shown in figure 2. To solve this issue, new auto-initialization calibration logic has been developed for the GBT firmware. The phase alignment between the regenerated clock and the received clock is monitored to make sure that the data is sampled at the correct clock edge.

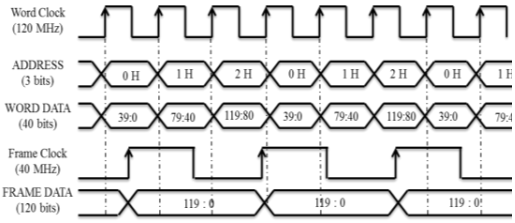

Fig. 2 Word Clock and Frame clock phase mismatch

Latency measurement is an important parameter in time critical communication. A detailed study of the latency measurement is done for all the possible combinations of the mode of operation. Measurement setup is shown in figure 3.

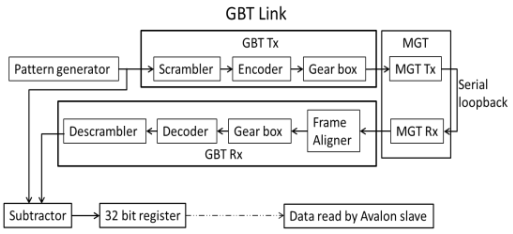

Fig. 3 Test setup for GBT link latency measurement

Altera Stratix-V provides an internal Temperature Sense Diode with built in 8 bit ADC to monitor the die temperature. A firmware module is developed to read the temperature value. Temperature stability analysis is also done for reliability testing of the design. For easy system integration of the GBT firmware, an Altera QSYS [3] framework wrapper is designed. Important features of the design like temperature, coding type, mode of operation, transmit and receive link data, state of Phase Locked Loop and the latency value in nanoseconds are integrated in GBT QSYS for ease of operation. Altera transceiver tool kit [3] is used to validate transceiver link signal integrity. The channel performance of the transceiver link in serial and optical loopback is studied by interpreting the eye pattern. Bit Error Rate (BER) analysis is done using a pattern generator and checker, to measure the performance with variation in coding scheme, optical link length and temperature variation.

Results and Conclusion

Transmission latency is measured for the possible combinations of mode of operation for Transmitter and Receiver section and tabulated as shown in figure 4

Tx Standard	Tx Standard	Tx Latency Optimized	Tx Latency Optimized
Rx Standard	Rx Latency Optimized	Rx Standard	Rx Latency Optimized
450 ns	350 ns	200 ns	150 ns

Fig. 4 Latency measured for GBT Link

Signal quality of the GBT protocol operating at 4.8 Gbps is measured using a wide bandwidth high end Lecroy serial data analyser. Eye diagram is shown in Figure 5. Eye Width is 176.8 ps, Eye Height is 373 mV and BER of 5.525×10^{-12}. The data obtained are acceptable and beneficial for further studies. Results in detail will be presented.

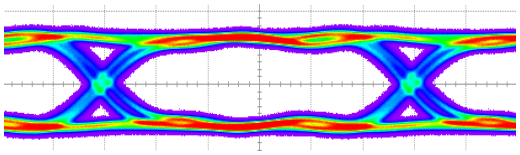

Fig. 5 Eye Diagram for the GBT Link testing on Altera Startix-V

Acknowledgement
Authors like to thank Shri Vaibhav Baid of Berylline Labs for his kind help and cooperation.

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[3] Stratix-V Device handbook volume 1 Altera