Comparative Analysis of tapped delay line architectures used in time stamping

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Introduction

Time stamping [1-3] is a technique used for measurements of time interval as well as single-hit and multi-hit time at high hit rates. This technique is implemented with the help of tapped delay line (TDL) [1]. This paper elaborates the comparative study of two developed architectures of TDL, used for time stamping a 'hit' signal with 150 ps resolution using reference clock period of 20 ns. The implementation of both architectures is carried out using standard cells of 0.35 µm CMOS process and the design issues are presented.

Time stamping of hit using TDL

The TDL is realized by a chain of cascaded 'N' buffers each with delay 'T_d' such that reference clock period $T_{ref} = T_d \times N$. It provides N delayed replicas of clock each separated by time interval of T_d, which determines the resolution of time stamping over a range of clock period. The arrival time of 'hit' is stamped by determining the number (N_f) of delayed clocks till its occurrence. The value of N_f multiplied with 'T_d' gives stamped time of hit signal with respect to the previous rising edge of clock. In order to determine 'N_f', meta-stable hard D flip-flops are used for sampling and as data storing element. Two architectures developed have been analyzed and compared vis-à-vis.

First Architecture (clock samples hit)

In the first architecture of TDL (Fig.1(a)), the rising edges of delayed clocks stamp the status of 'hit' signal and store the data into N-bit register. When 'hit' signal leads the M^{th} ($0 \leq M \leq N$) delayed clock, the corresponding flip-flop is set to logic-1 state (Fig. 1(b)). The post $(M+1)^{th}$ to N^{th} delayed clocks set the remaining flip-flops to logic-1 state. The output of register is N-bit thermometer code, where the first logic '0-to-1' transition count 'M' (provided by thermometer decoder) is N_f.

A transition of the last bit Q_N of register is used as end of conversion (eoc) signal. It stops further stamping of 'hit' signal corresponding to next clock cycle by disabling either delayed clocks or D flip-flop. However, in both the ways, the processing logic has timing path delays higher than 'T_d' and is uncontrollable across process and operating condition variations. This overwrites the first few bits of thermometer code by the new stamped values of 'hit' signal (Fig. 1(b)). Thus, this architecture is not suitable to measure the arrival time of hit with respect to previous rising edge of clock.

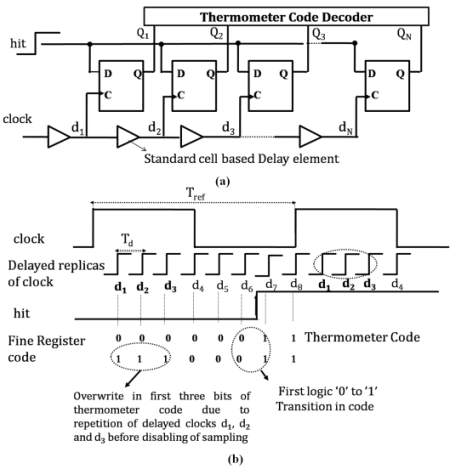

Figure.1. First Architecture of TDL (a) Schematic (b) Timing Diagram

Second Architecture (hit samples clock)

In the second architecture of TDL (Fig. 2(a)), the 'hit' signal stamps the state of delayed clocks and stores the values in register. The functionality of this architecture is explained for

N (=8) number of delayed clocks $d_{N\ (N=1\ to\ 8)}$ covering the range of one clock period (Fig. 2(b)). The count corresponding to first logic '1' to '0' transition in the register code gives N_f. The register code corresponding to various arrival times (t_1 to t_6) of hit is shown in Fig.2(b). To detect the first logic'1' to '0' transition, a transition detector based on magnitude comparison between two consecutive bits of register code is designed and implemented.

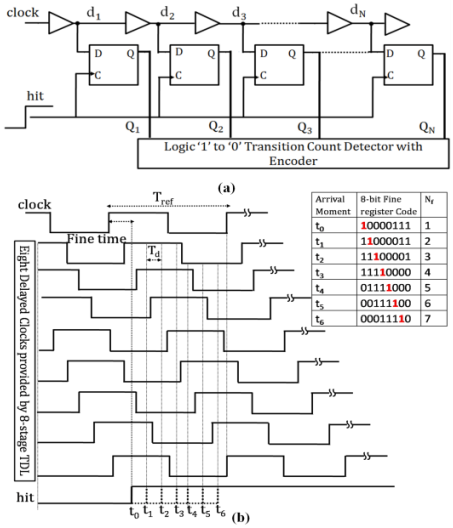

Figure.2 Second Architecture of TDL (a) Schematic (b) Timing Diagram

Simulation Results

The performance of TDL architectures is tested using Verilog test bench. To verify the issue of code over-write in the first architecture, a hit signal at time 1.9 ns from previous rising edge of clock is applied. Due to the processing delay of 1.5 ns (including 500 ps Clock-to-Q delay, 800 ps buffer delay for eoc and 200 ps gate delay), first 11 bits of thermometer code are overwrite, (Fig.3(a)). Using second architecture, the logic transition detected by the transition detector is at position 12, which multiplied by 150 ps gives the hit arrival time of 1800 ps. The linearity of second architecture of TDL is verified by applying linear sweep patterns of hit in steps of 300 ps with respect to clock over 20 ns range. Fig. 3(b) shows the plot between measured relative times of hits versus applied time steps on typical corner. The maximum INL is 90 ps and DNL error is less than 150 ps.

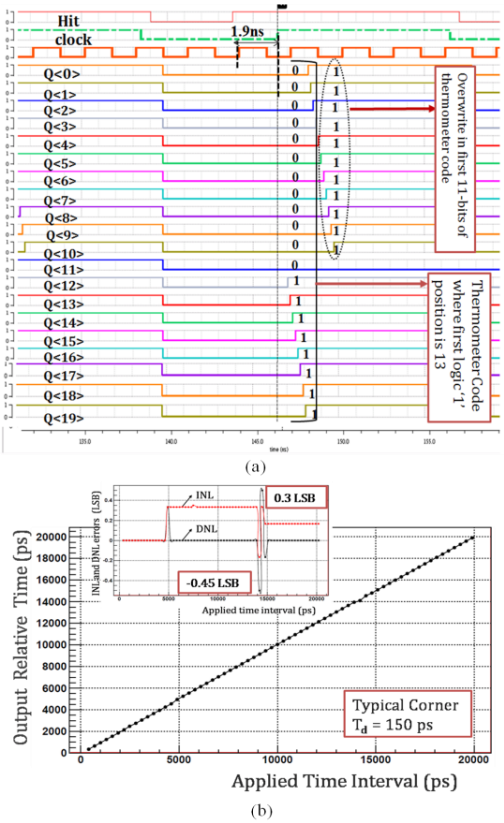

Figure.3 (a) code overwrite in first architecture (b) Linearity of time interval characteristics of second architecture

References

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