Total Ionizing dose studies of CMOS Structures in 0.35µm CMOS Technology

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Introduction

Radiation hard and low power circuit is pre-requisite in particle physics experiments, electronics for space and nuclear reactors [1]. Low power consumption of CMOS technologies therefore attracted many particle physics experiments [2, 3]. The main issue in using CMOS readout frontends is its degradation of performance and failure in radiation environments. Conventional CMOS devices (Manhattan) supported by Process Design Kits (PDK) are radiation soft, limiting their use in these applications. Edgeless devices are reported to be radiation hard but are not supported by PDK's of many foundries. This paper presents the study and design of different transistor structures, degradation of its parameters at different Total ionizing dose (TID). This paper also reports the accuracy of foundry supplied SPICE model by comparing measured and simulated transistor characteristics, conformal mapping is used to map edgeless transistors into their Manhattan equivalent [4].

Design of Radiation Hard Structures

A pilot test chip 4.3mm X 2.3mm consisting 88 test structures, binned up-to 35um for single finger and 110 um for edgeless devices were designed and fabricated in 0.35um commercial CMOS process. Fabricated test chip were packaged in six sets of 44 PIN PFM package for irradiation and characterization. The test structures was part of this study were Simple Manhattan geometry, Extended gate, Gate all around, Modified gate around ,Enclosed gate devices, Waffle geometry devices

Typical layouts of test structures are shown in Figure 1. Manhattan devices are default devices supported by both foundry and CAD tools. Radiation hard by layout technique standard is Enclosed gate devices [5] but customized CAD tool and foundry support is required for circuit simulation and extraction of non Manhattan devices.

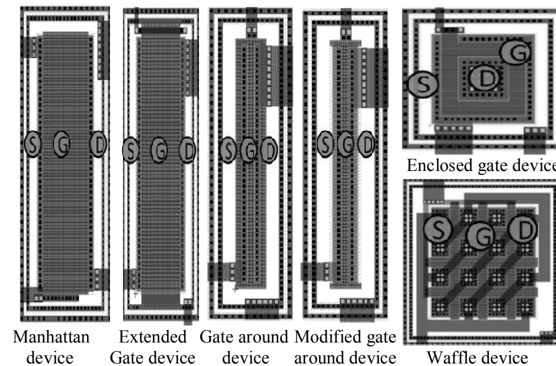

Figure 1 Test structures

Gate around devices and modified gate around devices are novel layouts which are edgeless but are still like Manhattan structure. These novel devices can be easily mapped into their Manhattan equivalent; these are also unique in the sense that they solve the minimum aspect ratio limitation of Enclosed gate devices and have comparable radiation hardness capabilities.

Irradiation and Characterization

Gamma irradiation for packaged devices was carried out using Co-60 based gamma chamber at dose rate of 410rad(Si)/min up to TID of 1.5Mrad(Si) in eight incremental steps.

Test devices are characterized for I_d-V_d, I_d-V_g, V_{th} , I_{sub}-V_g, I_{on}-I_{off} slope and C-V characteristic at each TID step(variables used have usual meaning). Conformal mapping is used to map Aspect ratio of edgeless devices into their equivalent Manhattan.

Result of Irradiation Studies

In this study Manhattan and Extended gate structures degrades considerably reaching 200

krad(Si) maximum as reported in Figure 2.a. Gate around and modified Gate around devices do not show considerable degradation up-to 1.5 Mrad(Si) as reported in Figure 2.b. Enclosed gate devices are superior to all other families for TID tolerance, they show good tolerance up-to 1.5 Mrad(Si) as reported in Figure 2.c. Waffle devices show marginal superiority w.r.t. Manhattan structures. Electrical characteristics of gate around have very marginal difference w.r.t. Manhattan devices. Silicon measured Vs SPICE model variation is 10-15% as reported in Figure 3

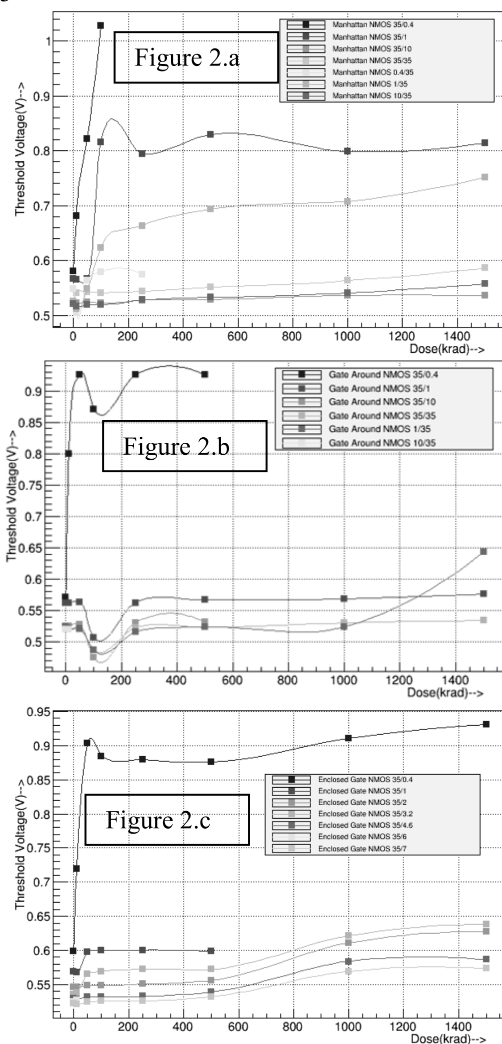

Figure 2 Threshold voltage variation w.r.t TID Manhattan devices (a), for Gate around devices(b) and for Enclosed gate devices(c).

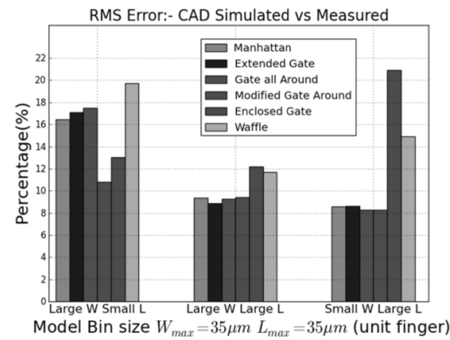

Figure 3 RMS error for Simulated Vs Measured characteristics after conformal mapping

Conclusion

0.35um CMOS technology using Manhattan transistor can be used safely up to 100krad(Si). With use of edgeless devices 0.35um technology can used safely up to 1.5 Mrad(Si) for both novel Gate around and Enclosed gate structures.

Design carried in conventional Manhattan structure can be mapped to gate all round by changing single mask providing novel way to get radiation hardness in conventional CMOS process.

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