Development of high gain photodiode array based on commercial CMOS process

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Introduction

Design of monolithic photo sensors in standard CMOS technology is a trend over the years. Although, commercial CMOS process poses a some constraints on designing photo sensor, but at the same time induces more design challenges by ruling out any scope of modification in any process steps which are basically optimized for circuit design. On the other hand co integration of sensor and electronics on the same wafer offers an edge over the hybrid system as the parasitic introduced by the external connections bring about degradation of system performance in terms of diminished sensitivity and speed.

Developing photodiodes in commercial CMOS process and integrating it with readout electronics without any process modification involves formidable challenges. Due to low resistivity of the wafer used in commercial CMOS process, the junction capacitance per area of the PN junction is quite large thereby limiting the size of the active area of the photodiode leading to degradation in high speed response. On the contrary, the sensitivity and quantum efficiency of the optical detector tends to improve with increase in active area of the detector. The major challenge in designing high gain photodiode in sub micron CMOS technology is to avoid the premature perimeter edge breakdown or the soft breakdown. This paper reports two different design approaches of high gain photodiode arrays in commercial 0.35 um CMOS technology and HV CMOS process.

Design of high gain photodiode structure in 0.35 um CMOS process

High gain photo diode structures have been designed and developed in standard 0.35 um CMOS technology. These structures are based on P+/N-well junction as an active area. To avoid the premature edge breakdown, N-well based virtual guard ring around the active area has been used. Beside that poly control gate is also implemented in two structures to enhance the breakdown voltage and also to minimize the probability of premature edge breakdown even further. As the devices are biased above the breakdown point quenching resistors are used to restore the devices back below the breakdown point after onset of avalanche phenomenon each time. Both the active and passive quenching methods are explored in different test structures. The prototype structures are co-fabricated in the ASIC ANUPAL (TDC) [1].

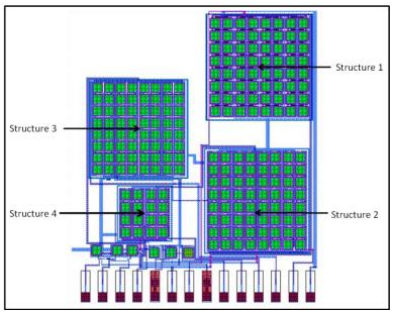

Fig 1: High gain photodiode structures in 0.35 um CMOS technology

Four different photo structures as show in fig. 1 have been designed with different geometrical spacing between the active area and the guard rings. The novel high gain photo diode structures based on the P+/N-well junction are blue enhanced as the nature of junction is shallow. First three structures are of 1 sq mm of area while the fourth one is of 0.25 sq mm.

Design of high gain photodiode structure in 0.35 um HV CMOS

Standard High Voltage CMOS process offers more design flexibilities towards the designers such as providing more number of wells of different depth, doping densities and also with higher breakdown voltage compared to the standard low voltage CMOS process. Nine different structures are designed and implemented in 0.35 um HV CMOS process.

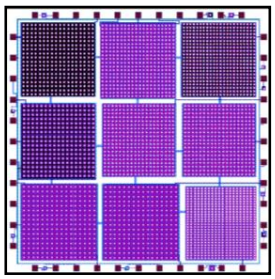

Fig 2: High gain photodiode structures in 0.35 um CMOS technology

Four different types of structures such as P-well guard ring, N-well guard ring, substrate guard ring, Deep N-tub/ P-tub based structures are implemented with different type and value of quenching resistors.

Test setup and Characterization

Characterization of the CMOS technology based high gain photo diode test structures are carried out with two different readout boards. One of them is the ANUSPARSH-II ASIC board designed and developed by ED, BARC [2] and the other one is the commercially available fast amplifier unit developed by CAEN. The devices are characterized by shining an ultra low light intensity LED from a commercially available LED driver coupled through optical fiber to the photo device. A Special optically transparent epoxy has been applied to ease the handling and also guiding the light efficiently towards the active surface area of the photo structures.

The device, readout electronics along with the LED driver and the optical fiber setup has been put inside a dark box and response of the novel photo structures were observed by changing the LED dial setting. All measurements are in low frequency mode of the BLUE LED thereby providing few photons at the end of the fiber.

While the devices in 0.35 um commercial CMOS process initiates showing optical response around LED dial position '4'(few hundreds of photons) , the structures in 0.35 um HV CMOS process shows much early detection around '2.9' of the LED dial setting (few tens of photons). This implies that the devices of HV CMOS process are having higher optical gain, and is estimated around 10E+5 @ 405 nm. This later structure is proved to be a promising structure for making SiPM, which is under development.

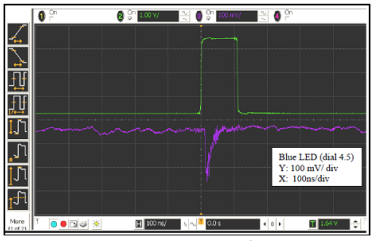

Fig 3: Oscilloscope response of the novel photo structure in 0.35 um CMOS process.

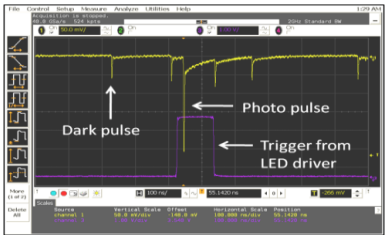

Fig 4: Oscilloscope response of the novel photo structure designed in 0.35 um HV CMOS

References

[1] K Hari Prasad, M Sukhwani, Pooja Saxena, V.B.Chandratre, C K Pithawa "Standard Cell based time to digital converter ASIC", Springer Conference Proceeding VCASAN, 258, 2013

[2] Menka Sukhwani, V.B.Chandratre et al "ANUSPARSH II": Front end readout ASIC for resistive Plate Chamber Detector", NSNI conference Proceeding 2013