In-house work on characterization of pixel chip pALPIDE

T. Sinha[1],* A. Biswas[3], A. Roy[4], D. Das[2], Dipankar Das[1] and S. Chattopadhyay[1]
[1]*High Energy Nuclear and Particle Physics Division, Saha Institute of Nuclear Physics, Kolkata - 700064, INDIA*
[2]*Applied Electronics Section, Saha Institute of Nuclear Physics, Kolkata - 700064, INDIA*
[3]*Department of Physics, Sikkim Manipal Institute of Technology, East Sikkim - 737136, INDIA*
[4]*Department of Physical Scciences, IISER, Kolkata – 741246, INDIA*
* *email: tinku.sinha@saha.ac.in*

Introduction

The activities of Muon Forward Tracker (MFT) for ALICE Upgrade had been started in the beginning of 2015. In this International collaboration, among 13 participating Institutes, the mechanical and the electronics technicians/engineers along with the scientists of Saha Institute of Nuclear Physics (SAHA) and Aligarh Muslim University (AMU) will constitute the Indian Collaboration [1].

The physics programme of ALICE using MFT will be started after the Long Shutdown 2 (LS2). The physics investigation will be devoted to high precision measurements of hard probes (heavy flavour hadrons, quarkonia, photons and jets). The MFT will allow ALICE to extend the precision measurements of the heavy quark resonances.

The MFT detector will be put upstream of the absorber of the MUON spectormeter i.e. much closer to the Interaction Point (IP) to add vertexing capability. The Si-tracking detectors of low-material budget will be used in MFT. The basic detection element of the MFT is the pixel sensor which is based on the CMOS monolithic pixel sensor technology.

The India-MFT collaboration will be focusing on two areas. 'The Pixel Characterization Work' and 'The fabrication of Water-Cooling system of MFT detector'. In this report, we will discuss on 'The Pixel Characterization Work'.

The Pixel Characterization Work

We had received w17-17 pALPIDEV2 chip made with pixel sensor of 30 μm epitaxial layer thickness and corresponding DAQ board from MFT collaboration in August, 2015. The procurement of hardware and handshaking between hardware and software took three months to formulate a test bench to study the pixel characterization of this chip. The testing of the chip was started from December, 2015 at SAHA, Kolkata. The update of progress of the work had been regularly presented in 'WGX Pixel Characterization' collaboration meetings.

Testing of pALPIDEv2 Chip

The size of the chip is 15 mm x 30 mm. The 524288 number of pixels were accommodated in 512 rows and 1024 columns of 32 regions of four sectors.

The testing of chip was done in two steps.

i) The threshold and noise distribution in four sectors of the chip had been studied with and without back-bias.

ii) Chip testing with ^{55}Fe source with and without noise masking.

The chip with the DAQ board was kept in a black box to avoid the exposure of light on the chip since light exposure worsened the threshold response. The dc 5.0 V was applied to chip as power supply and the current was set at 0.300 A. The chip was also tested in three back-bias -1.0 V, -2.0 V and -3.0 V with current set up at 1 mA, 6 mA and 10 mA respectively. The current consumption was almost 10 mA putting back-bais -3.0 V for this chip. So, this chip could not be tested up to the maximum value of back-bias i.e. -6.0 V as other collaborators performed.

i) The ***Threshold scanning*** (for 1% pixel) was done for the chip at different VCASN varying the I_{THR} values 10 to 100 in the step of 10 without back-bias. The VCASN values were applied from 45 to 75 in 5 intervals. I_{THR} and VCASN values were taken in DAC units. The purpose of the threshold scan is to determine the

signal threshold that is needed for a pixel to be hit. The threshold scan performs analogue injections using a programmable charge is injected into the preamplifier of DAC board. The injections are looping over the charge ranging from 0 to 50. By increasing the I_{THR} one can increase the threshold and vice versa. By increasing the VCASN however the effect is inverted and the threshold is decreased. The mean and root mean square (rms) values of all threshold and noise plots had been done.

The adjoining picture Fig. 1 shows the threshold and noise distribution of pALPIDEV2 chip along with the set up.

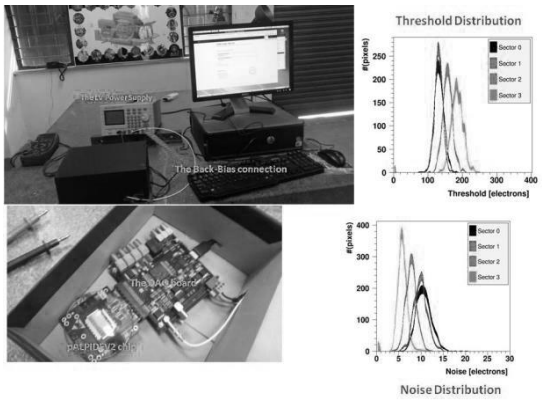

Fig. 1 Set Up for Pixel Characterization Work

ii) The ***Source Scanning*** of the chip with ^{55}Fe source of 8 mCi strength was performed without back-bias for 10^7 Trigger events. The chip was kept at four different distances from the source as 1.5 cm, 5.5 cm 8.5 cm and 12.0 cm respectively. This testing was done with and without noise masking. The hitmap and clustermap of the chip was analyzed from this scanning.

Results

The clustermap had been analyzed using cluster finding algorithm for 10^7 events. The hits on pixels are processed by this algorithm. A cluster is defined by either a single fired pixel or a group of fired pixels. The group is always considered as consecutive pixels, in horizontal or vertical direction. The number of clusters were found from this study and for each cluster, the number of hit pixels i.e. the cluster size was investigated. The Fig. 2 shows the cluster size for 10^7 events.

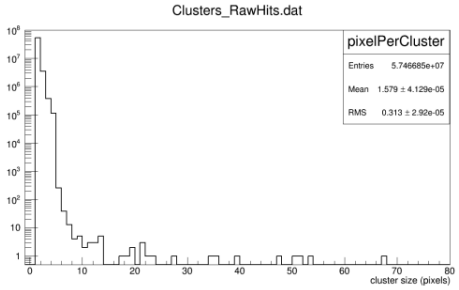

Fig. 2 The cluster size for 10^7 events

Hence, a comparison of the cluster size as a function of I_{THR} has been given in Fig. 3 for source to chip distances at 5.5 cm and 8.5 cm respectively.

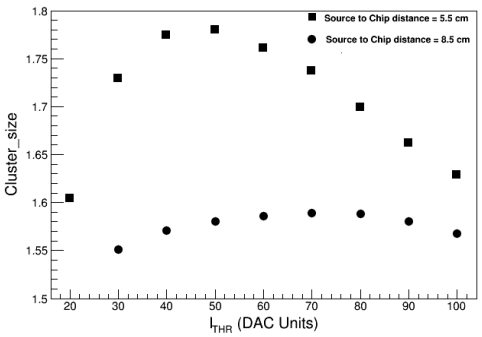

Fig. 3 Cluster size varies with source to chip distance

As the distance from the source to chip decreases, the chance to hit more pixels will be increased.

The study of the characterization on pALPIDEv2 chip is almost finished. The investigation on the performance of pALPIDEv3 chip is going on. An expertise has been developed during this pixel characterization study in different laboratories of MFT collaboration which will be utilized at the time of detector fabrication of MFT in future.

References

[1] Technical Design Report: ALICE-TDR-018, January, 2015.