Electronic Data Aggregation Architecture for High Energy Physics Big data taking Experiments

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Introduction

In the field of high-energy physics (HEP) experiments, a huge amount of data is produced at a very high rate. Over the years with the increase in the beam energy and luminosity, the aggregate data taking volume has increased substantially. To cope up with the increasing demands in data management, the HEP experiments now require a dedicated *data processing block* that can be used as a multipurpose data traffic manager. The common task of this block involves balancing of data distribution over multiple interface links, handling of time stamping for both trigger and trigger-less data traffic, distribution of fixed latency trigger or it might also act as a control instruction moderator block before forwarding control information to the detector.

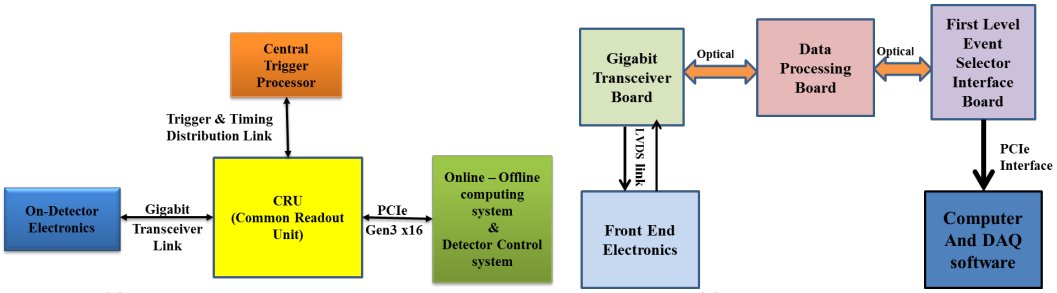
VECC is a participating member for engineering design of detector data flow manager for two major HEP experiments. One is CRU (Common Readout Unit) hardware design for ALICE Detector in RUN 3 at CERN, Geneva [1] and other is Data Processing Board (DPB) for Muon chamber (MUCH) detector of CBM experiment at FAIR, in Darmstadt, Germany [2]. In this article we try to highlight the similarity in between the two data readout architecture and also the expanding role of reconfigurable hardware in HEP experiments.

Purpose for using Reconfigurable Board

The readout data in HEP experiment is transferred from detector situated in harsh radiation zone to the data acquisition electronics located in the non-radiation area. The interface link standard used for data transmission must have very high reliability, can able to maintain fixed latency with error detection and correction capability. To match this specific requirement, CERN Electronics team have developed a unified protocol called GBT (Gigabit Transceiver). Soon it was realized that the number of sub-detectors using it is much more, and this requires many highly expensive optical GBT links. Hence, new ideas emerged to minimize the cost by multiplexing the trigger and control data transmission over a single link that gives birth to a new protocol called PON (Passive Optical Network). It uses both Time Division and Wave Division Multiple Access for data multiplexing. GBT and PON are two such interface links connecting the *data processing block* with the detectors [3].

The processing boards are connected to computing units over the commercial links for easy maintenance. Popular interface link standards at HEP experiments in recent years are PCIe (Peripheral Component Interconnect Express) with x16 lanes and 10G Ethernet standard. The former one connects directly to the PCs and the latter one to LAN card directly, or via a router. The designers also need to take care to keep up with the present trend in interface standard up-gradation, which is around 2-2.5 years cycle.

It would be a highly effective design solution if these processing boards use reconfigurable hardware like ultra-low power high-performance FPGA(s). It has many advantages like faster development time, no upfront non-recurring expenses (NRE), more predictable project cycle and field reprogrammability. Physicists who were running operations over offline raw data, can now push those common optimization algorithm to the hardware, that can do it real-time giving a speed up factor of at least 1000 times. As for example in CBM experiment different algorithms like micro slicing (time based data sorting), clustering are initially planned to be used directly in the computing node now uses FPGAs.



(a) FPGA Based Data Concentration Unit for ALICE Detector

(b) FPGA Based Readout Chain for MUCH Detector

FIG. 1: Showing a single block of electronic readout architecture

Application

In the ALICE experiment from Run3, is going for continuous readout architecture. It uses Common Readout Unit (CRU) as a central processing block for aggregation of data from multiple detector links over GBT and forwarding it to the computing firm over PCIe interface having x16 lanes. CRU will also participate in the trigger and timing information distribution from Central Trigger Processor to the detectors with fixed latency over TTC-PON links. It will also act as an intermediate managing node for the computing firm to provide a more robust and dynamic debug and control functionality for the experiment. An overview of CRU connection with its neighbouring blocks is shown in Fig. 1 (a).

In the CBM experiment different detectors like silicon tracking system (STS), MUCH, Ring Imaging Cherenkov detector (RICH) etc. will be used for different purposes. VECC is developing MUCH detector to detect low momentum muons generated from the decay of low-mass vector mesons in heavy-ion collisions.MUCH-XYTER that will be used as fontend electronics board (FEB) to capture data from GEM detector will be placed directly on the detector. MUCH-XYTER sends the data to the GBTx ASIC using differential electrical line at 320 Mbps. One DPB (Data Proccessing Block) can receive data from maximum four GBTx board and send data to backend First level Interface Board (FLIB) through 10 Gbps optical link. DPB also distribute global synchronization clock using white rabbit protocol to the full read out chain. For internal monitoring of registers in DPB and GBTx chip, IPbus protocol over Ethernet will be used. DPB connection overview is shown in Fig. 1 (b).

As can easily be seen that in both the architecture the processing blocks (CRU, DPB) got very similar interface link requirement and also resembles in functionality. So, in the development of firmware a joint effort has been made to make it generic and hardware independent for re-usability of such designs.

Conclusion

The data acquisition facility in VECC is using 20 nm Silicon Technology Altera Arria 10 FPGA for CRU (Common Readout Unit) block design at ALICE Detector in CERN, Geneva and 28 nm Silicon Technology Xilinx Kintex-7 FPGA for Data Processing Board (DPB) for CBM experiment at FAIR, Darmstadt.

References

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