Design and development of a front-end preamplifier for bolometric detector

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Introduction

A tin cryogenic bolometer detector is being developed to study neutrinoless double beta decay (NDBD) process [1]. The key elements of the detector are a neutron transmutation doped (NTD) Ge sensor, which is cooled down to 10 mK in a cryogen free dilution refrigerator (CFDR). Usually the NTD sensor (resistance ~ 500 MΩ at 10 mK) is driven using a constant current in the range of femto ampere to pico ampere. Whenever any incident photon/charged particle hits the absorber, the change in temperature is detected by the sensor and the corresponding electrical pulse is amplified and processed. In the present system, the electrical signal of the sensor is brought out of the cryostat using twisted pair cables and the signal is amplified using a low noise, high gain differential amplifier. One of the drawbacks of placing the front-end amplifier at room temperature is the use of long cables connecting the sensor to the amplifier at room temperature. The large cable capacitance along with the high resistance of the sensor gives rise to a problem of signal integration. The long cables connected to the high impedance sensor node are also very much prone to the external noise pickups. To enhance the signal to noise ratio and to minimize the signal integration due to long cables, a better option is to keep a pre-amplification stage in one of the intermediate stages of the CFDR closer to the sensor [2] as depicted in Fig. 1. Generally, a pre-amplification stage is implemented using a Si JFET, configured in unity gain source follower topology, and it is kept in one of the intermediate stages of CFDR. The preamplifier

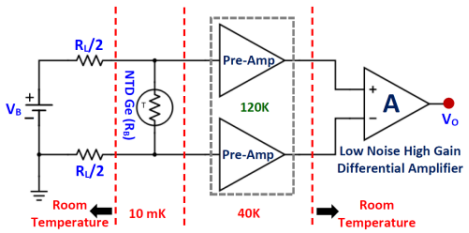

Fig. 1 Basic circuit schematic for cryogenic bolometer detector. Here the bias voltage V_B in series with high load resistor R_L (~ 20 GΩ) acts as a pseudo constant current source

is held in a thermal environment with an optimum temperature of around 120K.

In this paper, we present the design and development of the preamplifier for NTD sensor readout in a cryogenic bolometer. Initial testing of the preamplifier is done at room temperature and its results are presented.

Circuit schematic of preamplifier

A DC coupled source follower amplifier is designed using a low noise silicon JFET 2SK208 as shown in Fig. 2. To achieve a very high input impedance, the sensitive input node of the amplifier is surrounded by a "Guard trace" to minimize the PCB surface leakage current. The guard trace is driven by the same voltage as the input node by connecting the output node V_{out} to the guard trace. The other important factor in the design of a source follower amplifier is to achieve a voltage gain close to unity, which depends on the load resistor connected at the source terminal 'S_1' of JFET Q_1. Initially we have used a passive load resistor R_S of 1 kΩ (shown by dotted connections) which results in a voltage gain of ~ 0.64 only. To make the voltage gain close to unity for a given bias condition, the

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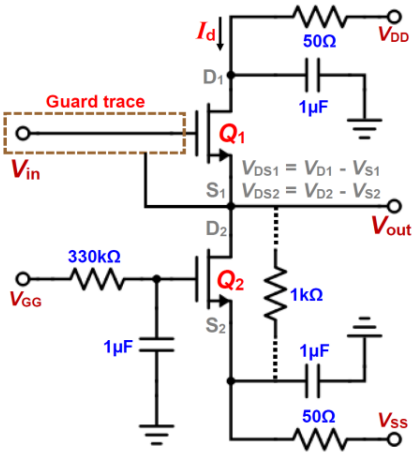

Fig. 2 Circuit schematic of preamplifier

value of the load resistor has to be kept high, however it will result in large power dissipation, a critical issue for cryogenic operation. Therefore, the passive load is replaced with an active load Q_2 in our design. The required DC supply for the amplifier is filtered using low pass RC circuit. The amplifier has been fabricated in-house in an FR4 substrate as shown in Fig. 3. Initial testing of the amplifier is done at room temperature. The frequency response of the amplifier is measured with passive load as well as active load. The DC biasing of the amplifier as well as measurement of frequency response in the band of DC–10 kHz is carried out using a PXI card interfaced with LabVIEW software. A LabVIEW code is also developed to automatically sweep the frequency of the input signal for acquiring the frequency and amplitude data of amplifier's output. For measurements above 10 kHz, a signal generator and a Tektronix oscilloscope is used.

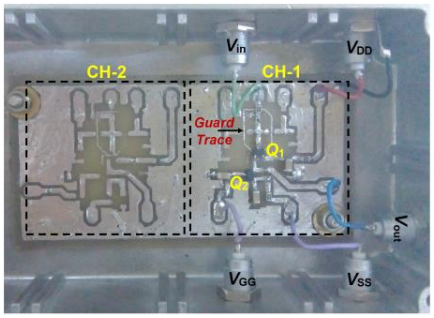

Fig. 3 Fabricated PCB with one optional channel

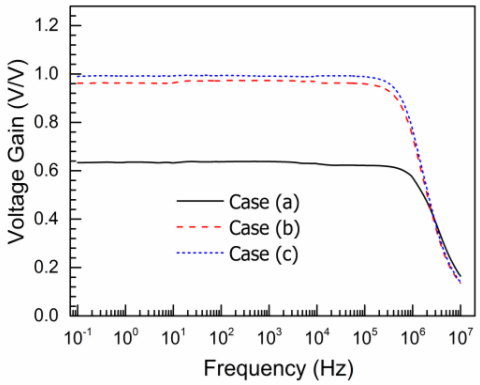

Fig. 4 Measured frequency response (a) with 1kΩ load resistor: I_d=1mA, V_{DS1}=1V (b) with active load: I_d=0.5mA, V_{DS1}= V_{DS2}=1V (c) with active load: I_d=0.5mA, V_{DS1}= V_{DS2}=2V

Table 1: Voltage gain and power dissipation for different conditions of operations

	Case (a)	Case (b)	Case (c)
A_V (V/V)	0.635	0.962	0.992
P_d (mW)	2.100	1.025	2.025

Results and Discussions

The frequency response is measured at room temperature with three different operating conditions as shown in Fig. 4. A voltage gain of 0.635 is achieved with a passive load resistor in Case (a). Replacing the passive load from the active load enhances the voltage gain to 0.962 with an operating 'I_d' of 0.5 mA only as shown by Case (b). Also the power dissipation reduces by 50% (Table I). Increasing 'V_{DS1}' and 'V_{DS2}' to 2V helps in achieving almost a unity voltage gain (A_V = 0.992). Therefore, an active load (Case-c) helps in achieving a unity voltage gain with almost the same power dissipation as in passive load condition (Case-a). A 3-dB bandwidth of DC – 2 MHz is obtained in all the cases which is sufficient for our application. The detailed noise characterization and testing of the amplifier at 120K is in progress.

References

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