Development status of Common Readout Unit at India for the ALICE detector at CERN

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Introduction

In order to extend the physics reach of ALICE and other experiments, the LHC is planning for an upgrade of beam energies and beam luminosities during Long Shutdown-2 (LS-2) in the year of 2019 and 2020. The increase in luminosities and hence the interaction rates helps to collect high statistics of data and sustain the advance research in state-of-the-art High Energy Physics (HEP) experiments. It will allow the ALICE detector to inspect the measurements of rare probes. After the LS-2 of LHC, the third phase (Run-3) will start in the year of 2021 with much higher beam luminosities. The luminosities for Pb-Pb collisions at center-of-mass energy of 5.5 TeV will increase from the present value of $10^{27} cm^{-2} sec^{-1}$ to $6 \times 10^{27} cm^{-2} sec^{-1}$ [1]. The maximum readout rate of the present ALICE TPC detector is 500 Hz of Pb-Pb events, but the overall goal for Run-3 is to readout 50 kHz Pb-Pb collisions and 200 kHz p-p and p-Pb collisions. The high interaction rate will result in a dataflow of ∼3.3 TB/sec from the detectors to the Data Acquisition (DAQ) system. This is a major challenge for the experiment. To handle this high data rate; the upgrade of detectors, their readout electronics and the DAQ sysem in ALICE have been planned since the year 2014. The Common Readout Unit (CRU) is an integral part of the detectors and the DAQ upgrade.

CRU acts as an interface to the on-detector Front End Electronics (FEE), trigger and the DAQ system. The CRU as a hardware is identical for all the constituent detector systems in ALICE. However, the firmware for each CRU is sub-detector specific depending on the physics requirements. The data from the sub-detectors are distributed among various CRUs. CRU has to perform versatile functionalities due to which it is implemented as reprogrammable board based on state-of-the-art 20nm Intel Arria-10 FPGA.

CRU Implementation Aspects

The ALICE CRU hardware framework depends on a solution where the CRU is directly plugged in to the PCIe slot of the DAQ servers. The ALICE collaboration made a joint venture with LHCb experiment for the custom developed hardware known as PCIe40 DAQ engine [2] as shown in Figure 1. It is a

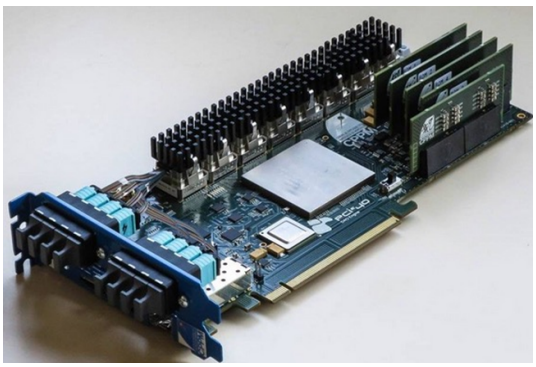

FIG. 1: CRU for ALICE detector.

PCI Express form factor based readout board. CRU is equipped with 130 high-speed communication links and consumes a peak supply current of up to 60 A. It has a high density interconnect PCB with more than 1750 components on it; with peculiar requirements of PCB material to support high rate data transmission with minimum distortion. CRU is a 14 layer board with a thickness of 1.57 mm (tolerance of 10%). Also there are laser drills re-

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quired for its fabrication. It has blind, buried and the stacked vias. Power requirements are supported by five mezannine cards.

Interfaces of CRU: The different system level requirements of the experiment are replicated to the protocol selection of the three interfaces of CRU. Gigabit Transceiver (GBT) protocol [3] is used for the interfacing on-detector electronics to CRU. It is a radiation tolerant, error resilient and bidirectional optical link data communication standard having fixed latency support for HEP experiments. The trigger interface to CRU is based on the Timing-Trigger and Control over passive optical networks (TTC-PON) [4]. TTC-PON standard is chosen for this interface as it has the high split ratio having fixed latency. The PCIe Gen3 x16 lanes (8 Gbits/s for each lane) interface is the most viable solution chosen for the sever side interface of CRU. This architecture is compact with no optical links and cabling at the DAQ servers.

Prototype tests and the production

Total 06 nos. of prototype boards were produced from three different production/assembling houses. 04 nos. of the prototype boards are already tested and verified at VECC Kolkata; delivered to CERN for integration tests with the detector front end. This step also served as a survey for the eligible companies to participate in the mass production of ∼300 CRU boards for the ALICE. All the produced, tested and verified CRU boards need to be delivered by the start of the Run-3 of ALICE.

Extensive tests are carried out at VECC for the verification of the developed prototype CRU hardware to ensure the reliability of the boards. Tests are performed at the fabrication stage as well as the basic electrical performance measurements are done. The boards are subjected to the temperature cycling tests at the fab house to omit the possibilty of soldering issues. X-ray test is also performed after the FPGA with 1932 pin BGA package is mounted on the PCB to avoid any shorts between the adjacent ball points. The produced prototypes are configured for the first use and tested for the functional verification of its communication interfaces for the qualification of the prototypes at VECC. FPGA basic functionality test, memory read-write test, port read write tests are performed. The card is inserted into a server computer for the PCIe card identification. It will drive the tests and store the results as well as the board information in server. I2C interface tests are performed to detect the PLLs, different on-board ICs, temperature monitoring and other peripherals. Optical transceiver links are tested using the data loopback tests at 4.8 Gbps (GBT transmission rate), both internal and external loopback tests are performed. The transceiver links are tested for trigger transmission at 10 Gbps. The 16 lanes of the PCIe interface are detected in PC and the data transmission functionality test of each lane are successfully done. Each lane of PCIe gives the throughput of ∼6.9 Gbps due to the protocol overhead. The transceiver optimization technique [5] is also applied to reduce the losses occuring due to the high data rates of the transmission. The detailed results will be presented.

References

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