Prototype development of VME 64 standard general purpose 6U module and its application for Timestamping

Ram Kumar Paul, Pintu Maity, Partha Dhara,* and Ayan Banerjee
Computer Division, Variable Energy Cyclotron Centre, Kolkata - 700064, INDIA
** email: partha_dhara@vecc.gov.in*

Introduction

The user customizable VME modules, which are available in market are mostly processor based, where VME IOs are handled by the processor chip and response time is slow.
This paper will describe the design and development of a FPGA based VME 64 standard general purpose 6U module and its application for timestamp sharing. This module has front end SFP port for high speed optical communication to other module. The module will also serve as development platform to implement any user level logic for VME board. The module also has future scope for attachment of mezzanine board for further extension of input processing.

Hardware design

The four major building blocks of this module are power supply unit, frontend IOs, backend VME IOs and FPGA as main programmable device. The VME design block schematic is shown in Fig.1.

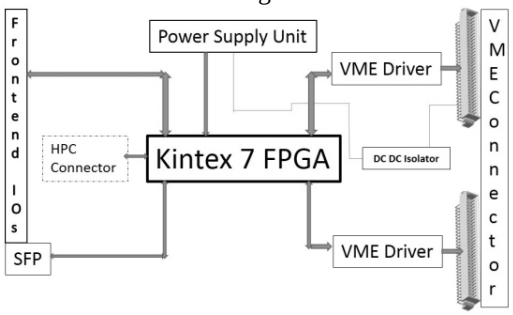

Fig. 1: VME board design schematic.

The physical dimensions of this module is as per VME 6U unit. The schematic design is done in house using Altium PCB design software and this is a total 8-layer PCB. The FPGA is Xilinx Kintex 7 FPGA, part no XC7K160T-FBG676. The dimension of this FPGA is 27mm x 27mm and total pins are 676. This FPGA have logic resources of 25,350 slices, 1, 62,240 logic cells, 2, 02,800 CLB Flip flops and which are enough to accommodate VME design and user design.
The FPGA needs total six different power supply to six different IO banks. So plug in type power supply boards have been designed and fabricated as shown in Fig. 2.

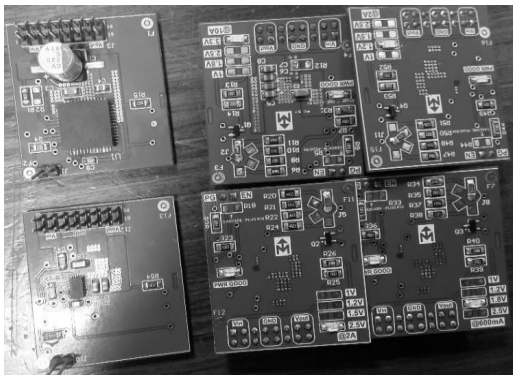

Fig. 2: VME board Power supply units.

The fully soldered ready to use VME module photograph is given below Fig. 3

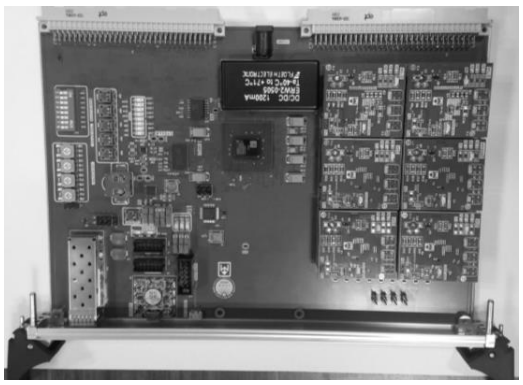

Fig. 3: general purpose VME 6U module

Firmware design

The firmware has been designed using Xilinx ISE design tool and VHDL language for the FPGA. The VME IP core has been procured and integrated with the board. The firmware has been designed to use this as a VME slave module with front end optical communication for timestamp sharing with other module for heterogeneous DAQ application. The RTL schematics of the design are given below figures

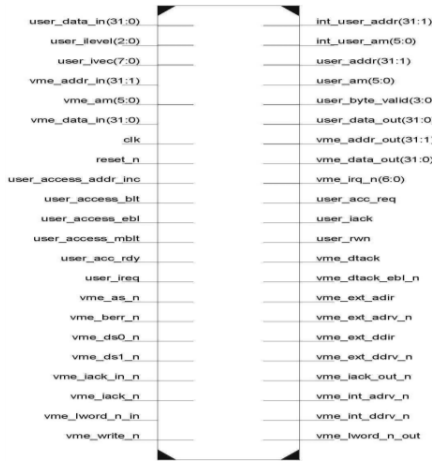

Fig. 4: RTL schematic of VME IP

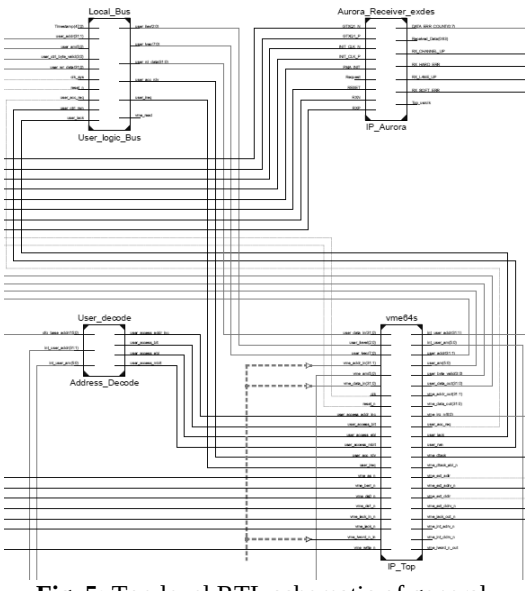

Fig. 5: Top level RTL schematic of general purpose VME 6U module

The block marked as User_logic_bus in Fig. 5, can be customized by the user to implement their own design. The VME part is handled by VME64s block and aurora receiver is responsible for optical communication.

Experimental results & timestamp sharing

VME read, Write access has been tested with this general purpose VME module and an experiment has been carried out with this as timestamp receiver module. Timestamp is being used to correlate the events within heterogeneous Data Acquisition System [1], [2]. The experimental set up is given below Fig. 6.

Fig. 6: Timestamp experiment with general purpose VME module

Conclusions & future scope

This general purpose VME module is completely indigenous design and user customizable FPGA resources with frontend optical IO connectivity. This module also has future scope for HPC connector for attachment of VITA 57.1 standard mezzanine board for further extension of input processing

References

[1] Ram Kumar Paul et al., "Prototype VME & CAMAC form factor Timestamping module development for Nuclear Physics experiment", DAE-BRNS Symp. On Nucl. Phys. 60 (2015), p.922-923.

[2] Ram Kumar Paul et al., "Heterogeneous data acquisition system & time correlation," 2017 8th ICCCNT, Delhi, 2017, pp. 1-3. doi: 10.1109/ICCCNT.2017.820403.