Development of large-area silicon detector on indigenously grown high resistivity wafer

Sourav Mukhopadhyay[1,3],* V.B.Chandratre[1,3], Kalyan Bhanja[2], and Sameer S Shinde[2]
[1]Electronics Division, Bhabha Atomic Research Centre, Mumbai - 400085, INDIA
[2]Heavy Water Division, Bhabha Atomic Research Centre, Mumbai - 400085, INDIA
[3]Homi Bhabha National Institute, Anushaktinagar, Mumbai - 400094, INDIA
* email: souravm@barc.gov.in

Introduction

Silicon is the widely used semiconductor material in developing high-resolution detectors for applications like nuclear physics, high energy physics experiments, radiation safety & monitoring system. However, commercial wafers are expensive and not easily available as there are only a few manufacturers across the globe to grow detector grade silicon crystals. Heavy Water Division, BARC has taken an initiative to grow high resistivity detector grade silicon crystal ingots to fulfil DAE's need for this crucial material.

To validate and qualify the wafers as detector grade material, Electronics Division, BARC has developed a large area silicon pad sensor using the indigenously grown high resistivity 4-inch silicon wafer. The detectors have been fabricated at Bharat Electronics Limited (BEL), Bengaluru, and preliminary tests have been carried out at the wafer level for the first batch of processed wafers.

Design of large-area silicon detector

Silicon detectors of various size and geometry, similar to a proven design [1] earlier fabricated on a commercial wafer, has been accommodated inside a 4-inch mask layout. A design of a large area 6x6 array of silicon pad detectors with ~ 1cm^2 individual pad size has been placed at the centre of the wafer. At the periphery, designs of various baby (test) detectors like photodiodes of square and circular geometry, pixel array detectors (PAD) with different array and individual pixel size are placed. Fig.1 shows the picture of a processed 4-inch wafer.

The salient feature of a high-resolution silicon detector in radiation detection and spectroscopy systems is the low leakage current to achieve optimum signal to noise ratio. Hence, the large area silicon detector was designed with multiple floating guard rings (FGR) along the periphery of the 6x6 silicon pad, while the individual pad geometry is optimized as square type with rounded corners to avoid premature edge breakdown at a lower voltage. Furthermore, additional gettering process steps were introduced during the detector fabrication to ensure a low leakage current.

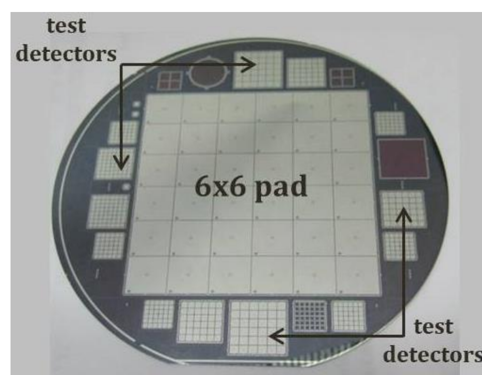

Fig. 1 A processed indigenous silicon wafer.

This design of the silicon pad sensor consists of four mask sets, i.e., P+, contact, metal and passivation-layer-opening, which are used to define the P+ regions, contacts, metallization and openings in the passivation layer. It is a "P on N" type design where the starting wafer is N-type, and a P type dopant is implanted from the top to form the P-N junction. For the packaging purpose, individual pad connections are brought

through metal routing lines to the wire bonding pad sites at the periphery.

Wafer specifications

The indigenously grown high resistivity N-type wafers, on which the detectors were fabricated, has the following salient features, as shown in Table 1.

Table 1: Wafer specifications

Sr No.	Parameter	Value
1.	Wafer size	4-inch
2.	Wafer thickness	500 ± 25 µm
3.	Polishing	Double-sided
4.	Lifetime	600 µS
5.	TTV	~ 28 µm
6.	Orientation	<111>

Characterization of the silicon sensor

Electrical characterization was carried out at the wafer level to determine the operating parameters of the pads [1]. Current versus reverse voltage (I-V) and detector junction capacitance versus reverse voltage (C-V) measurements of all the individual pads of the first batch of processed wafers have been carried out. Fig.2 shows the uniformity plot of the leakage current (measured at a reverse bias of 100 V) among the pads of the best performing wafer so far. Fig.3 depicts the corresponding geometrical mapping of the 'good' and 'bad' (w.r.t. the leakage current) pads in that particular wafer. Fig.4 shows the capacitance-voltage response of a few of the pads.

Results and Discussion

Initial results were promising (leakage current is within the acceptable range at the operating voltage) in most of the pads, while it is a bit on the higher side in a few others. Full depletion voltage is ~ 80 V. Detailed tests are going on. Characteristic uniformity among the pads in a wafer has to be improved to enhance the production yield of the large area detector. Processing of subsequent batches of indigenous wafers is currently underway at the foundry. With enhanced wafer processing and better handling, improved results are expected as the quality of indigenously grown ingot is good.

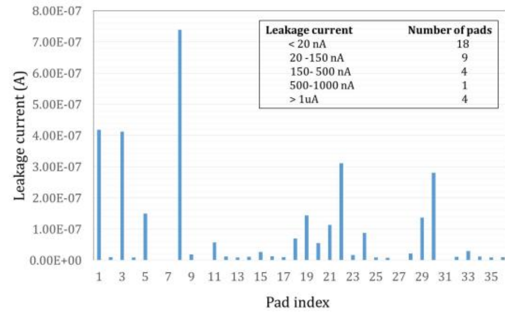

Fig. 2 Uniformity of the leakage currents.

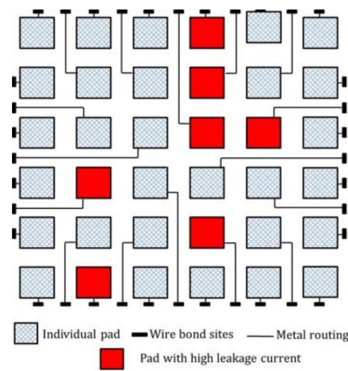

Fig. 3 Mapping of the 'good' and 'bad' pads.

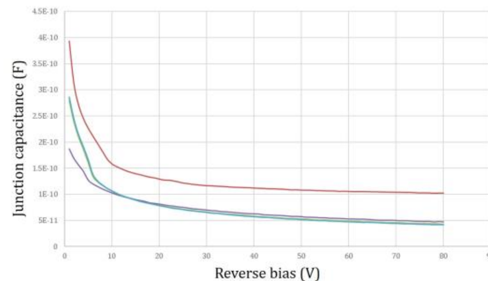

Fig. 4 C-V curve of the individual pads.

Acknowledgement

We want to thank Ranjay Laha, Arijit Das, of Bharat Electronics Limited (BEL), Bengaluru, for fabrication support.

References

[1] S. Mukhopadhyay, V.B.Chandratre et al. 2021 JINST 16 P09026