Development of high resolution Pulse Shape Discriminator Circuit for Particle Identification using indigenously developed monolithic CMOS based Timing Discriminator

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Introduction

In the recent years, VECC has developed and tested successfully a Multichannel CSA and Shaper ASIC (VECC002) for the energy measurement of alpha (1-40 MeV) and proton in Granular charged-particle Multiplicity-filter Detector Array (GMDA). As this detection of particle will be carried out in coincident with gamma rays, particle identification capabilities have to be incorporated in the signal processing chain of GMDA. The inherent capability of CsI(Tl) detector in identification of particles is being utilized in GMDA for identification of alpha, gamma, proton etc. However, the conventional method of pulse shape discrimination [2] using the method of obtaining the ratio of the late-time charge deposition to the total deposition suffers from low Figure of Merit (FOM) especially in the lower energy region. The ZCT (Zero-Cross-Over-Timing) technique is considered as the best method for particle identification (PID) as it is independent of detector time resolution. However, higher FOM of ZCT method depends on the time resolving power of the timing discriminator circuit. For CsI(Tl) detectors, the difference in decay time constants of output for different particles corresponds to different rise times in pre-amplifier output. It has been identified from the experimental data that this property can be exploited for efficient pulse shape discrimination at lower energies using a timing discriminator circuit with time resolution around tens of picosecond.

The development of a high resolution timing discriminator circuit in sub-micron CMOS technology has been undertaken for this purpose. The design details of this circuit has been described in the subsequent section followed by the design of a high resolution Pulse Shape Discriminator (PSD) using the same timing discriminator. The simulation results to discriminate particle having difference in rise time of approximately 700 ns have been shown in the following section.

Design of high resolution Timing Discriminator

The block diagram of the high resolution timing discriminator circuit is shown in Fig. 1. The whole circuit has been implemented in CMOS. This circuit essentially follows the theory of a constant fraction discriminator (CFD) to generate a time pick-off pulse which is independent of rise time and amplitude of the input. However, the design artifacts due to the non-ideal parameters of the CMOS circuitry introduce timing jitter in the CFD output. Due to these limitations, the time resolution achieved by commercial timing discriminator modules is of the order of hundreds of picoseconds.

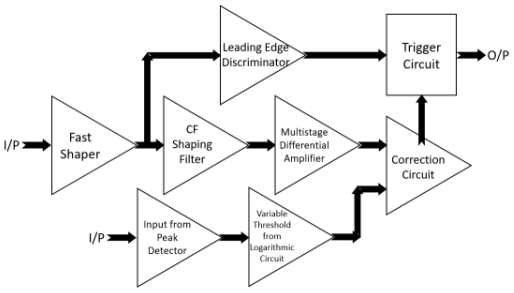

Fig. 1: Block Diagram of Timing Discriminator

In this design, the non-ideal parameters have been identified mathematically and with the help of design simulations, an additional correction circuit has been introduced in the design. It has been observed that a variable threshold generated from a tunable logarithmic circuit can reduce the time jitter further, and time resolution of the order of tens of picosecond can be obtained. The main challenges in this design are to achieve the required tuning parameters for the logarithmic

circuit for its use in different applications and making the logarithmic circuit work at higher count rates. The simulation result is shown in Fig. 2 for amplitude variation from 100 mV to 1 V. The maximum deviation of zero-crossing time is within 10 ps.

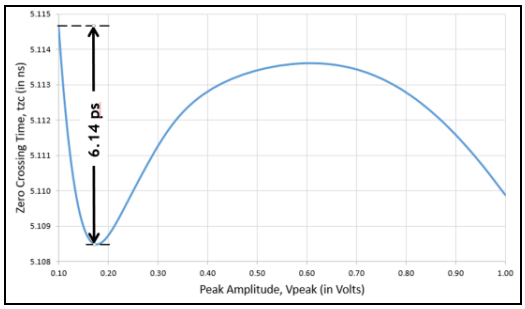

Fig. 2: Time resolution obtained from the high resolution Timing Discriminator

Design of Pulse Shape Discriminator Circuit using Timing Discriminator

Based on the design of the timing discriminator described in the previous section, Fig. 3 shows the high resolution Pulse Shape Discriminator circuit for particle identification. In this method, two discriminators with amplitude walk of the order of tens of picosecond have been integrated. One of them is configured as independent of pulse amplitude but dependent on rise time of the input pulse by adjusting the constant fraction delay time in the shaping circuit shown in Fig. 1. The other discriminator is configured as independent of both the amplitude and rise time.

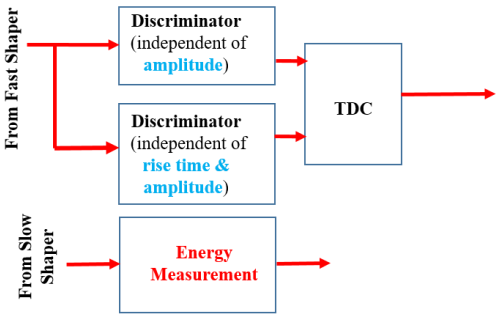

Fig. 3: High resolution Pulse Shape Discriminator

Fig. 4 shows the simulation result of detection of pick-off time using the circuitry described in Fig. 3 for two different particles (alpha and gamma). The amplitude walk for both the particles is confined to 10 ps. The pick-off time for both the particles are spaced apart due to difference in rise time of the input pulses. It is evident that the identification can be carried out with high value of FOM which cannot be achieved using conventional pulse shape discrimination method and electronics for CsI(Tl) detectors.

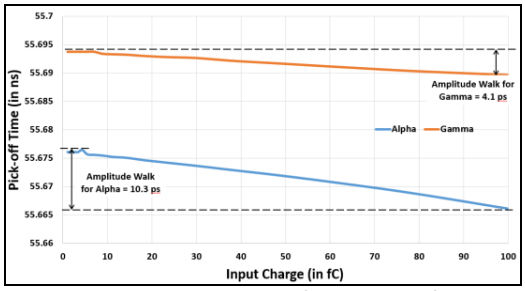

Fig. 4: Simulation result of detection of zero-crossing time of two lower energy particles with higher FOM

Conclusion

The high resolution timing discriminator circuit has shown excellent performance for pulse shape discrimination at lower energy levels. Further work has been undertaken to improve the design of logarithmic circuit by increasing the dynamic range of the tuning parameters of logarithmic circuit and to increase the count rate of the overall circuit. The final design will be utilized with VECC002 ASIC for the GMDA detector to implement a full-fledged system.

References

[1] Manish Kumar Jha et al., "Development and testing of Front End Electronics (FEE) for Granular charged-particle Multiplicity-filter Detector Array (GMDA) using VECC-002 ASIC", "65th DAE-BRNS Symposium on Nuclear Physics" 2021.

[2] Y. Ashida et al., "Separation of gamma-ray and neutron events with CsI(Tl) pulse shape analysis", Prog. Theor. Exp. Phys. 2018, 043H01