Design, Development and tests of real size PCBs for 3rd station readout at CBM-MuCH

Shuaib Ahmad Khan[1,2],* Jogender Saini[1], Ekata Nandy[1], Rajesh Ganai[3], Anamika Pallavi[1], Zubayer Ahammed[1,2], and Subhasis Chattopadhyay[1,2]
[1] *Variable Energy Cyclotron Centre, 1/AF Bidhan Nagar, Kolkata 700064, INDIA*
[2] *Homi Bhabha National Institute, 1/AF Bidhan Nagar, Kolkata 700064, INDIA and*
[3] *Department of Physics, University of Calcutta, 92, Acharya Prafulla Chandra Rd, Kolkata, West Bengal-700009.*

Introduction

The Compressed Baryonic Matter (CBM)[1] is an upcoming experiment in the future Facility for Anti-proton and Ion Research (FAIR) in Darmstadt, Germany. The CBM experiment will have various detector systems. The Muon Chamber (MuCh) is a sub-system of the CBM experiment among others like Silicon Tracking System (STS), Ring Imaging Cherenkov detector (RICH) etc. The detector system in CBM is composed of a segmented absorber system with detectors placed in between. MuCh consists of four detector stations sandwiched between the absorber segments. At the 3rd and 4th stations of MuCh; Resistive Plate Chambers (RPCs) have been conceived for muon tracking as a cost-effective technology option. Here we report the design, developemnt and tests of the paded structure readout PCBs for the 3rd station of the RPC detector.

Design concept for the real size PCB of RPC detector

The trapezoidal shaped signal pickup PCB for the actual size of the 3rd Station of the RPC detectors at CBM-MUCH is designed with precise calculations. These detector readout PCBs are of 4-ft (about 1143-mm) in length and 2-ft (about 543mm) wide and 2.4mm thick. Total 18 no. of modules accommodate the full azimuth coverage with segmentation of 20 degree for each detector module and 2 degree for each individual PAD[2]. Each PCB is designed using trapezoidal pads layout with progressively increasing radius in the 48 no. of concentric circles. The size of the smallest trapezoid pad is 1.01cm and that of the largest pad in the farthest most radius (annular ring from the beam interaction point) is 5.0 cm as shown in Figure 1. The precise calcualtion of parameters are crucial for the integration of the designed PCBs with the MUCH-XYTER[3] based front end electronics (FEE) and with the other detector systems at the experimental site. To produce the trapezoidal shaped readout boards exact calculations could be carried out using the method of mathematical calculus or the concept of engineering drawing could be used. The calculations include the replication steps, rotation angles, horizontal and vertical tolerances to avoid any shorts during the production. Here we have used the concept of engineering drawing for all the replication steps and placement positions. Designing of the PCB is carried out in Proteus software platform.

Development Methodology

The tolerance between the two pads both horizontally and vertically is 0.2 mm to avoid any shorts and kept such so that it could be produced in the production foundries with optimum charges. Provision is also kept for the injection of the external test pulse charge through capacitor coupling to the FEE boards. Total 04 no. of connectors with 1.27 mm pitch are placed for insertion of FEE boards at approximately equal distance. A space is left from the zeroth coordinate of the placement of the PCB; this solution

*Electronic address: shuaibkhan@vecc.gov.in

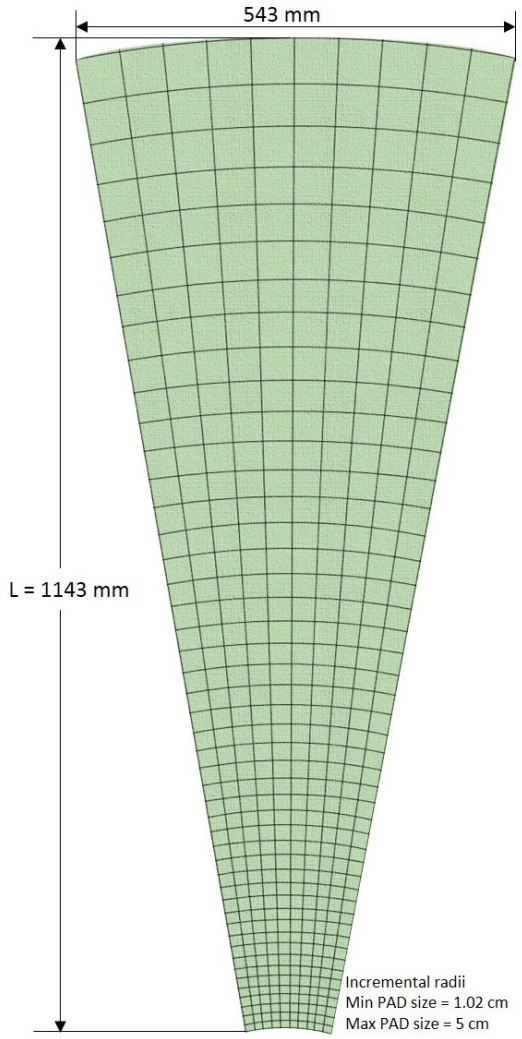

FIG. 1: Design of readout PCB for 3rd station at CBM-MuCH.

facilitates the placement of PCB in the test beam system also. The signal tracking of T8 size is chosen and routing is done with minimum 8 mil (1 mil = 0.0254mm) track to track distance and the broom shaped at the far end so as to avoid cross talk between the nearby signal tracks. The PCB is outlined with the through holes for screwing at the board edge to attach the pickup panels to the detector firmly for efficient charge collection. 02 no. of such boards are fabricated with flame retardant FR4 material, ENIG finish and Glass Trans Temp (Tg) 170 degree centigrade for production quality tests and to decide for the further production lot.

Results and Summary

2 no.s of PCBs are produced for the first test with the RPC detectors. The initial testing of the PCBs have been carried out in VECC. The produced PCBs are investigated carefully for any wobbling issues and continuity checks on the long and the short tracks. The charge collected by the pads on the PCB are transferred by the via-in-pad of 40 mil size to the component side of the PCB. The charge is coupled to the front end electronics through the surface mount device capacitor of 1 nanofarad of 0805 size. The data are being acquired via MuCh-XYTER FEE boards. Data are being transferred from the FEE to the FPGA based concentrator board where is data is processed and transferred further to the PC via the optical fibres through the Small Formfactor Pluggable (SFP) interfaces. The overall performance of the detector along with PCB has been tested successfully in GIF++ facility at CERN Geneva. As of today the RPC detector along with the designed PCB is under test at mini-CBM GSI, Darmstadt-Germany. Further results will be discussed.

References

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[3] Rafal Kleczek, Analog front-end design of the STS/MUCH- XYTER2-full size prototype ASIC for the CBM experiment, JINST 12 (2017) C01053.