Development and testing of RTL code for Prototype 8-Channel 500MSPS Digitization system

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Introduction

Waveform digitizers are essential readout instruments in nuclear physics experiments. It is always desirable to digitize analog signals at maximum possible sampling frequency with higher resolution maintaining very low baseline noise and utilize Digital pulse processing algorithms to extract vital information from the signal. Efforts have been put to design hardware to achieve highest channel densities to cater to large High Energy Physics Experiments. Various digital signal processing algorithms have also been implemented in FPGA and tested on custom 2-Channel 250MSPS digitizers [1] [2]. Firmware development to readout digitized data from such high density, High sampling rate digitizers involves deep understanding of latest SoC/FPGA architectures and state-of-the-art data transfer protocols between ADCs and FPGA to achieve high channel densities. JESD204B/C is the latest data transfer protocol incorporating up to 12.5 gpbs/15 gbps SERDES (serializers and Deserializers) with inbuilt CDR (clock data recovery) and Synchronization mechanisms across multiple ADCs.

In this paper, we present development of RTL code and its testing on ADC-FPGA evaluation module. It supports both external trigger readout and triggerless readout, accommodating the needs of low-rate full waveform readout and channel-independent low threshold acquisition, respectively. The system has two Quad Channel ADCs running at a sampling rate of 500 MSPS with 14-bit resolution for each channel.

Hardware Architecture

Two 4-Channel ADC Evaluation modules have been interfaced to a SoC/FPGA Evaluation module through High density - High Data rate cable which has FMC connector at both the ends. Two FMC Connectors on the SoC/FPGA Evaluation module provide connectivity to FPGA High speed SERDES pins. Reference clock for FPGA is provided from high performance, dual-loop, jitter attenuator clock generator Module optimized for JESD204B data interfaces.

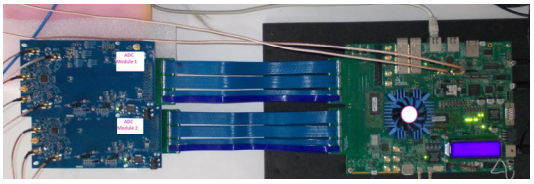

Fig. 1 : Experimental setup with ADC and FPGA Evaluation modules

Firmware Architecture

JESD204B interface describes a serial data Link between ADC/DAC and FPGA [3]. Each link may have multiple SERDES connections. ADC IC used in the current setup has two JESD204B links each catering to 2 Analog-to-Digital conversion cores in the IC. Two ADC Evaluation modules, each wired with one ADC IC are interfaced to the FPGA board. As there are 4 JESD204B links in the system, 4 JESD204B IP Cores are instantiated in the FPGA. For synchronous digitization, SYNC signal from all the IP Cores are passed through AND gate and a common SYNC_N signal is interface to all the ADCs. JESD204B link parameters for each link are arrived as L=2, M=2 and F=2.

Various clock signals internal to FPGA are required to be carefully selected so as to achieve best possible timing performance from the implemented RTL code. The current implementation has Device clock running at 983.04 MHz. This clock is divided by 2 inside ADC to achieve best timing performance and low Aperture jitter, thus achieving sampling clock as 491.52 MHz. Total 8 SERDES lines between both the ADCs and FPGA are initialized to work at

9830.4 mbps data rate. Suitable Link clock (245.76 MHz) and Frame clock (245.76 MHz) are chosen so as to capture proper data at MAC and Transport layer correspondingly. Figure 2 illustrates the block diagram of the implemented code.

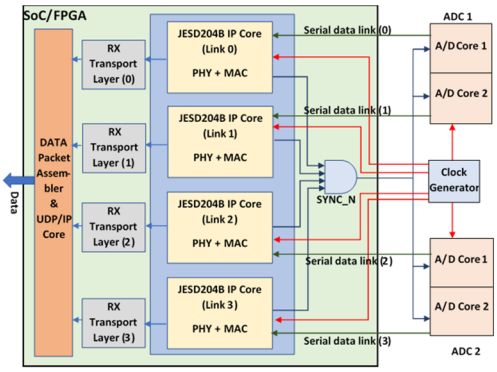

Fig. 2: Block diagram of the implemented design in FPGA

Result and Future scope

Complete code with 4 JESD204B links instantiated along with their transport layer has been compiled and synthesized in the SoC/FPGA design synthesis software. Analog input signals (20 MHz sinusoidal waveform) has been applied to 6 of the analog inputs. Essential clock signals are provided to Device clock inputs. The digitized waveforms have been captured in FPGA on-chip signal monitor/Analyzer tool as shown in the figure 3.

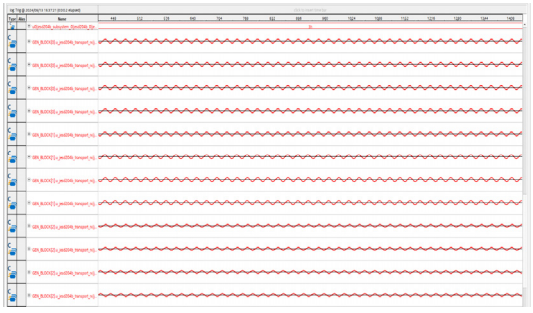

Fig. 3: Capture of 20 MHz sinusoidal waveform

Multilink synchronous 8-Channel digitization RTL code has been implemented & tested in FPGA. Various Digital pulse processing algorithms developed in-house and tested on 2-Channel 250 MSPS digitizer like Digital CFD, Pulse Shape Discrimination and Pulse height Analysis can be implemented in the FPGA firmware mentioned above, it will provide further enhancement to the capabilities of system.

References

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[2] "A real time digital CFD based DAQ system for high resolution nuclear spectroscopy" : "Krati , Saurabh Neema, Shibshankar Sikder, Saju Joy"; 67th DAE Symposium on Nuclear Physics (SNP-2023) Dec 9-13, IIT Indore, MP

[3] JESD204B Survival Guide, https://www.analog.com/media/en/technical-documentation/technical-articles/JESD204B-Survival-Guide.pdf