SEU mitigation technique by Dynamic Reconfiguration method in FPGA based DSP application

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Field Programmable Gate Array (FPGA), an SRAM based configurable devices meant for implementation of any digital circuits is susceptible to malfunction in the harsh radiation environment. It causes the corruption of the configuration memory of FPGA and the digital circuits starts malfunctioning. There is a need to restore the system as early as possible. This paper discusses about one such technique named dynamic partial reconfiguration (DPR) method. This paper also touches upon the signal processing by DPR method. The framework consisting of ADC, DAC and ICAP controllers designed using dedicated state machines to study the best possible downtime also for verifying the performance of digital filters for signal processing.

Introduction

In physics experiment nuclear pulses generated from various detectors have been processed / shaped by analog modules for better signal-to-noise ratio. A framework with a dipswitch as a fault injection system has been constituted to process nuclear pulses by realizing reconfigurable digital signal processing through FIR and IIR low pass filters in Xilinx FPGAs. The goal is to address both the dynamic reconfigurable flexibility of implementing various filters with the shortest reconfiguration time and the mitigation technique to enhance the reliability of the FPGA based hardware against Single Event upsets (SEU) and Single Event Functional Upsets (SEFU).

System Description

The circuit contains two channels for ADC1 and ADC2 inputs. It has a static area and a separate area called reconfigurable partition reserved for filter implementation.

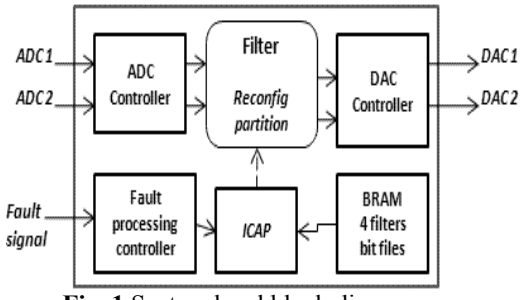

Fig. 1 System level block diagram

A dipswitch emulates the SEU fault injection system. The filter portion of the circuit is reconfigured upon receipt of the fault. Partial bit files for four different filters are generated following module based partial reconfiguration design approach. Analog signals having maximum 1.4 Vpp with rise time 40 ns and fall time of 1.2 us are sampled at clock rate of 100 MHz and fed to digital filters. Outputs of the filters are reconstructed using 16-bit DAC to verify the shaping performance of the digital filters. The FPGA based DSP framework has been designed, codified and implemented. The parts are as follows:

1) Signal processing chain (ADC-filter-DAC).
2) DPR architecture.

Signal Processing Chain

First stage of this chain consists of data-to-clock phase alignment module. In this module, the incoming ADC data output is sampled at four different phases of the clock period, and valid data has been captured at the appropriate clock. The second stage contains the *filter module*. Two direct form-FIR and two 1st order IIR filters configurations are implemented.

DPR architecture

Virtex4 and above family of FPGAs supports dynamic re-configurability fully or partially. DPR is the ability to reconfigure the

FPGA at run time without affecting the other logic. This sub-module consists of a partial reconfiguration controller, ROM module that holds the partial bit files of the filters and an ICAP primitive. The ICAP controller module manages the handshaking between the ROM memory and the ICAP. Upon receipt of the fault signal, reconfiguration is initiated.

Results

The pulse output profile information is tested with input 500 mV and 40 ns rise time. The output pulse rise time is 100 to 250 ns. The oscilloscope captures filter input/output as shown in figure 2.

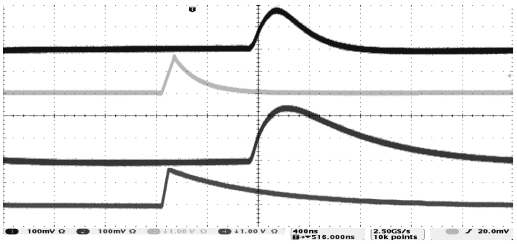

Fig. 2 IIR CH (1) IN/ OUT CH (2) IN/ OUT

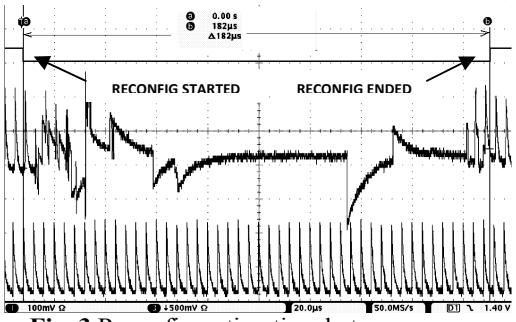

Fig. 3 Reconfiguration time between cursors

The partial bit file size for each filter is 70.97 KB. The reconfiguration time is 182 us w.r.t. ICAP (En) signal as shown in figure 3. During the reconfiguration period, the filter output gets distorted. It reconfigures to an IIR filter replacing the existing FIR filter dynamically as shown in figure 4 and 5.

Conclusion

To mitigate the effect of upsets in the firmware due to the effect of radiations, a run time reconfiguration technique called DPR have been successfully working in this framework with the configuration latency of 410 ns / frame.

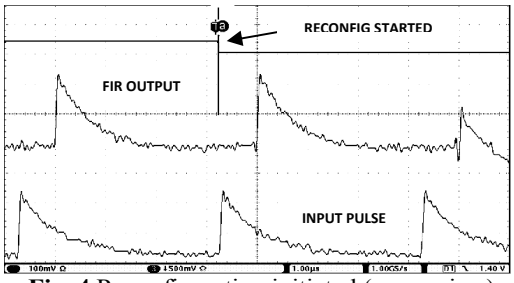

Fig. 4 Reconfiguration initiated (zoom view)

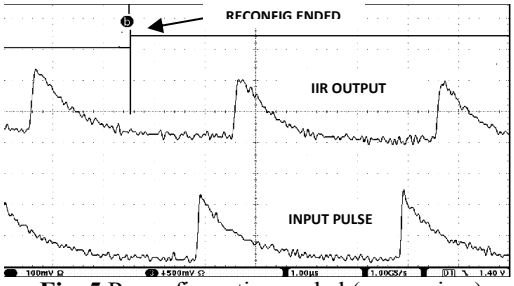

Fig. 5 Reconfiguration ended (zoom view)

The Virtex4 frame consists of 41x32= 1312 bits. A dedicated ICAP controller is designed to achieve one of the best performances.

References

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