Fast timing readout for silicon strip detectors

*A. Jhingan[1], N. Saneesh[1], M. Kumar[1], J. Vesic[2], B. R. Behera[3], S. K. Mandal[4], M. Gorska[2], P. Boutachkov[2], R. Ahuja[1], E. T. Subramaniam[1], H. Schaffner[2], P. Sugathan[1], N. Madhavan[1], I. Kojouharov[2], J. Gerl[2,5], H. J. Wollersheim[2]

[1]*Inter University Accelerator Centre, P. O. Box 10502, New Delhi - 110067, India*
[2]*Gesellschaft fur Schwerionenforschung, Planckstrasse 1, D-64291 Darmstadt, Germany*
[3]*Department of Physics, Panjab University, Chandigarh- 160014, India*
[4]*Deptartment of Physics and Astrophysics, Delhi University, Delhi - 110007, India*
[5]*Facility for Antiproton and Ion Research, Planckstrasse 1, D-64291 Darmstadt, Germany*
* *email: akhil@iuac.res.in*

Introduction

The development and performance of a 16 channel hybrid fast timing amplifier (FTA), for extracting timing information from silicon strip detectors (SSD), is described. The FTA will be used in a time of flight (TOF) measurement, in which one SSD is used to obtain the ion velocity (A) as well as the energy information of a scattered particle. The TOF information with a thin transmission SSD, acting as ΔE detector (Z) in a detector telescope, will provide a unique detection system for the identification of reaction products in the slowed down beam campaign of low energy branch (LEB) at NUSTAR-FAIR. Such a system will also provide large solid angle coverage with ~ 100% detection efficiency, and adequate segmentation for angular information. A good timing resolution (⩽ 100 ps) enables to have shorter flight paths, thus a closely packed 4π array should be feasible. Preamplifiers for energy readout in SSD are easily available. A major constraint with SSDs is the missing high density multi-channel preamplifiers which can provide both fast timing as well as energy. Provision of both timing and energy processing, generally makes circuit bulky, with higher power consumption, which may not be suitable in SSD arrays. In case of DSSSD, the problem was overcome by using timing from one side and energy from the other side. A custom designed 16 channel FTA has been developed for DSSSD design W from Micron Semiconductors, UK.

Fast Timing Amplifier (FTA)

The FTA has been fabricated using high frequency bipolar junction transistors (BJT). The design utilizes inverting three stage common emitter amplifiers with an emitter follower at the output stage. The circuit is inspired by the earlier developed design of Beeskow [2]. The schematic layout of the same is shown in fig.1.

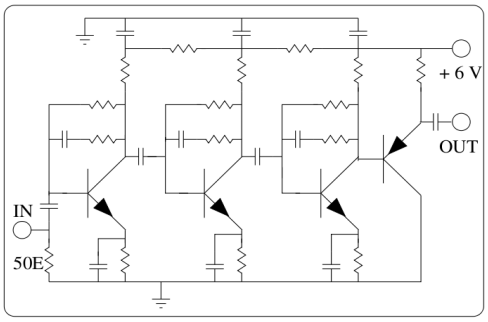

Fig.1 : Circuit diagram of FTA

The transistors are biased in collector feedback bias mode, and a negative feedback is provided for gain control and improved high frequency response. Table 1 shows the specifications of the FTA.

Table 1 : FTA specifications

No. of channels	16
Input signal polarity	Positive
Input impedance	50 Ω
Gain	50
Max. output voltage	- 1 V (50 Ω load)
Rise times	~2 ns (without detector)
Power requirement	1.6 W (100 mW/ch.)

The 16 channels were assembled on an 8 x 5 cm^2 FR4 board. There are 8 channels each on top and bottom side of the board. Each channel occupies a space of 2.5 x 1 cm^2. A 34 pin (17 pair) FRC socket is provided on the board compatible with DSSSD FRC pins. The DSSSD is directly plugged into this socket thus eliminating cables between FTA and DSSSD. Such a configuration improves timing performance, especially in case of thin

DSSSD, which have a very high capacitance. The timing outputs are driven by miniature coaxial cables (50Ω) to a specially designed flange, having sealed PCB based FRC feed-through for signal transmission. Thereafter the signals are fed to Phillips 715 CFD followed by TDC. FTA was designed to extract timing signal from the junction or *p*-side of DSSSD. To extract energy information, the *n*-side signals are fed to Mesytec charge sensitive preamplifier (CSPA) MPR-32 & shaping amplifier (SA) STM16 combination. Fig.2 shows the schematic of the readout scheme.

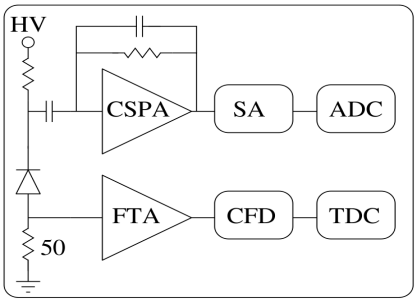

Fig.2 : Readout scheme of a single strip

Performance

The timing performance of the FTA with DSSSD has been evaluated in a scattering chamber at IUAC. The TOF of light and heavy ions were measured with respect to a micro-channel plate (MCP) detector (flight path ~ 15 cm). Fig.3 shows the experimental set-up with DSSSD plugged into FTA board and the MCP.

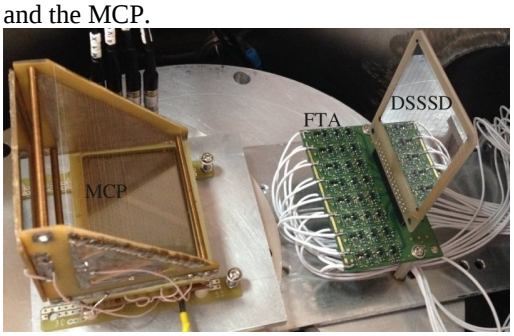

Fig.3 : TOF set-up with DSSSD and MCP

The system was initially tested with radioactive alpha emitters, and than using beams from Pelletron accelerator (IUAC) and UNILAC-SIS18 at GSI. The FTA was tested with SSDs of thickness 20 µm, 40 µm, 140 µm and 300 µm. Average resolution of about ~ 800 ps FWHM (pixel and energy gated) has been observed for 5.48 MeV α with 40 and 140 µm DSSSD, and 1.2 ns for 300 µm DSSSD. The rise times were 4 ns for 40 µm DSSSD. The time resolution of start MCP detector is about 200 ps for 5.48 MeV α.

At IUAC, an elastic scattering experiment was performed by bombarding a ^{197}Au target of 0.2 mg/cm^2 thickness with a 122 MeV ^{28}Si beam provided by the Pelletron accelerator at IUAC. The measurements were carried out in the General purpose scattering chamber (GPSC) and the detector system was installed at 60 degree with respect to beam direction. A rise time of ~ 6 ns and a pulse height of 300 mV was measured for the timing signal of the DSSSD. Fig. 4 shows the TOF spectrum of one strip with about 800 ps FWHM. On applying energy gate from *n*-side strip, a pixel resolution of about 240 ps is obtained. On subtracting MCP contribution, a pixel resolution of 170 ps FWHM is deduced.

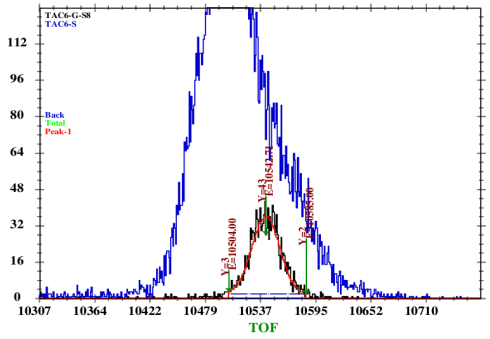

Fig.4 : TOF for one strip (blue) and energy/pixel gated (black).

The FTA was also tested with a 20 µm single sided silicon strip detector (SSSSD), with 16 strips and area 5 x 5 cm^2. The capacitance of the detector is ~ 1 nF per strip. A test measurement was performed with slowed down ^{124}Xe beam (~10 MeV/A) from UNILAC-SIS18 accelerator at GSI. For such a high capacitance detector, a rise time of 10 ns is observed with a pulse amplitudes of ~ 200 mV (for ~ 200 MeV energy loss). Data is being analyzed to extract timing resolutions of this SSSD with respect to MCP (start detector).

Acknowledgements

We acknowledge the help and support from Kusum Rani, R. Dubey, A. Yadav, Ruchi Mahajan, Meenu Thakur and Priya Sharma during the test measurements at IUAC.

References :

[1] Zeidmann et al., NIM 118 (1974) 361
[2] Lynen et al., NIM 162 (1979) 657