Design of Multichannel Readout ASIC for particle tagged gamma spectroscopy at VECC

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Introduction

Granular charged particle **M**ultiplicity filter **D**etector **A**rray (GMDA)[1] to be used for light charged particle (LCP) tagged gamma spectroscopy measurement at VECC have to handle 24 sections of 2x2 CsI(Tl) detectors, confined in a very small volume of the chamber to cover the 4π angle. Due to the low gain of the photodiode, coupled with the scintillator, Signal-to-Noise Ratio (SNR) for the front-end signal processing has to be very high in order to achieve equivalent energy resolution of the detector. Moreover, because of the very small volume of the chamber, unlike scattering chamber, heat dissipation of the associated front-end electronics should be in order of tens of mW per channel.

To mitigate all these problems in the development of the GMDA signal processing, the development of indigenous readout ASIC was undertaken as no such commercial ASIC was found to cater to this stringent requirements.

With this motivation, an 8-channel integrated ASIC consisting of a preamplifier and a fifth order Gaussian shaper was designed using 0.18µm SCL CMOS technology. The details of the design of the preamplifier and shaper are described in the subsequent sections followed by the results of the tape-out.

Design of the Readout ASIC

The design of the ASIC was mainly divided into two parts i.e. preamplifier and the Gaussian shaper. The critical specification in the design of the preamplifier was to detect of a low charge (in order of hundred fC) with an equivalent noise charge (ENC) in the order of the resolution of the detectors to ensure proper measurement of the energy of the detected light charged particles. Additionally, the power consumption of the preamplifier required to be kept sufficiently low to allow room for the shaper circuit which was more power hungry as compared to the preamplifier.

a) Preamplifier

The preamplifier was designed with standard single-stage folded-cascode topology followed by a source follower to have sufficient gain-bandwidth of the amplifier along with low output impedance to drive the shaper circuit. Figure 1 shows the schematic of the preamplifier. The total current through M2 was the sum of current through M0 and M1. The power consumption was optimized by separating M1 from supply voltage and keeping small current in the other branch.

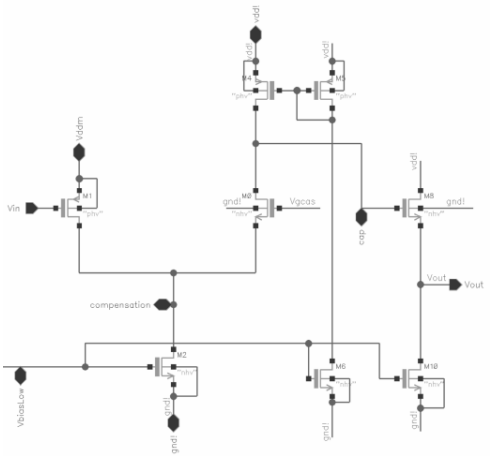

Figure 1 Schematic of *Preamplifier Circuit*.

The total noise, comprised of two major components i.e. flicker and thermal noise, was optimized by keeping M1 large and by adjusting the size of the other transistors accordingly without altering the overall power constraint.

b) Shaper

The shaper, the most complex part of the readout ASIC, was designed to have variable shaping time with controlling options. A fifth-order Gaussian complex-conjugate shaper [2] was implemented with one real and two complex conjugate pair of poles. A Pole-zero compensation circuit was placed in between preamplifier and shaper.

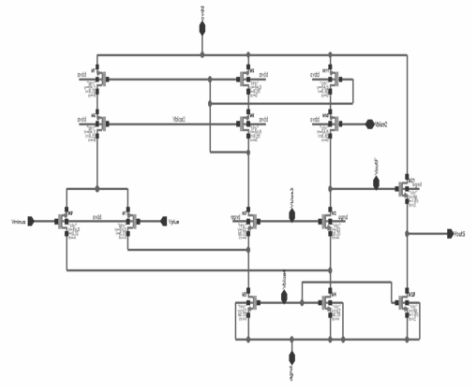

Figure 2 *Schematic of the amplifier used in FLF architecture.*

The follow-the-leader feedback (FLF) architecture [3] was used for the fifth-order filter as it is better suited for the design where sensitivity to changes in circuit parameters matter. Six separate amplifiers, five for five stages and one for feedback, were used in the design. Figure 2 shows the schematic of one amplifier. First stage of the FLF was for the real pole and next four stages are for the complex conjugate poles. Gain of every stage was optimized to give maximum dynamic range. Figure 3 shows the complete layout of the eight channel readout ASIC for the GMDA.

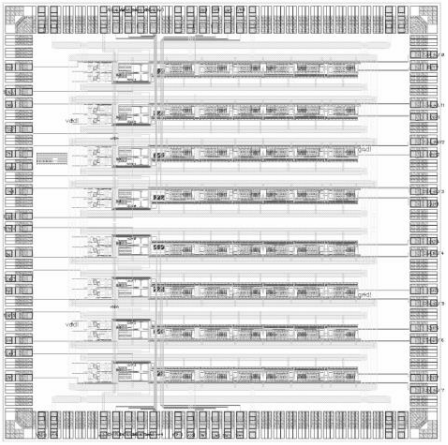

Figure 3 *The layout of the readout ASIC.*

Results

The simulation results as shown in Figure 4 was the typical output of the preamplifier and its shaped output with peaking time of 3μs. The overall ENC was within limit. The linearity and other specification were satisfactory as required in the application. It is important to mention that the test-bench prepared for testing of the tape-out considered all package parasitic of CQFP64 which was selected as the package of this ASIC.

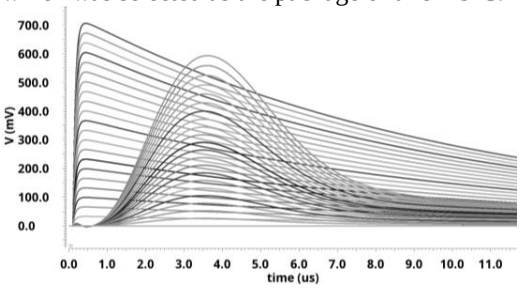

Figure 4 *The typical output of the preamplifier and shaper.*

Conclusion

The simulation results show that the design ASIC was suitable for the application of GMDA. The power consumption per channel, however, to be measured after fabrication of the ASIC.

References

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[2] S. Ohkawa, et al., Nuclear Instruments and Methods, vol.138, 1976, pp. 85-92.

[3] G. De Geronimo, et al., IEEE Trans. Nucl. Sci. vol. 47, no. 6, pp. 1857-1867, 2000