Design of CMOS peak detector for ASIC integrated with independent digital DAQ for nuclear spectroscopy

Manish Kumar Jha,* and Tanushyam Bhattacharjee
Variable Energy Cyclotron Centre, 1/AF Bidhan Nagar, Kolkata – 700 064
** email: mjha@vecc.gov.in*

Introduction

The data acquisition system for the experimental nuclear physics using cyclotrons at VECC relied upon CAMAC, VME backplanes along with use of commercially available hardware modules as the number of detectors used in the nuclear physics experiments were few in numbers. However, the modern experiments which were planned to be performed with a large number of heterogeneous detectors in order of thousands, these module based approach with VME and CAMAC as backplane are no more convenient [1] as the count rate handling capacity of the DAQ reduces to hundreds of Hz when number of channels increases. With this motivation, the development of FPGA based state-of-the-art independent digital DAQ with readout ASIC for the front-end electronics has been undertaken which will cater to the requirements of handling huge number of detectors with high count rate handling capability. It is important to mention that full digital signal processing circuit, bypassing the readout ASIC, is impractical as allocating an ADC per channel for simultaneous signal processing is neither cost-effective nor superior in terms of specification and resources [2].

The data flow of the overall digital DAQ system therefore needs to be derived as per the flow of the front-end ASIC. The first stage preamplifier followed by a shaper are the common blocks in the system. However, the configuration of the Peak Detect and Hold (PDH) circuit along with the readout determines the architecture of the rest of the digital DAQ system to handle thousands of detector channels with high count rate irrespective of the placement of the multiplexed ADC inside or outside of the ASIC.

The present paper discusses the overall architecture of the PDH and associated circuit and the design and characterization of the two-phase PDH in CMOS carried out using 0.18µm CMOS technology of SCL foundry.

Architecture of the FEE ASIC

Fig 1 shows the architecture of the PDH circuitry which can handle huge number of detectors operating for high count rate application. To understand let us consider a nuclear physics

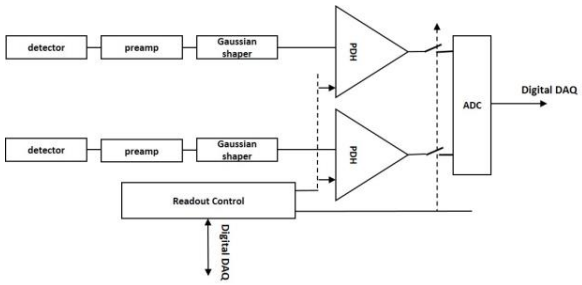

***Fig. 1** The architecture of PDH for digital DAQ*

experiment with number of detectors in order of thousand to be operated with a count rate of 20 kHz. A trigger based VME system with the best digitizer for such configuration will fail and can handle only less than a kHz count rate. However, the architecture as shown above can easily handle such count rate or more with the help of trigger-less, sparsification and derandomization circuits followed by FPGA based independent digital DAQ. The design of a two-phase PDH circuits will play an important role to achieve such an objective.

Design of the two-phase PDH

The PDH was designed to be operated in two-phase [3] as shown in Fig 2. During the write phase switches S1_W and S2_W are closed and other switches are open. The input voltage, $\mathbf{V_i}$ was applied on the negative terminal, $\mathbf{V_m}$ of the amplifier. The charging capacitor $\mathbf{C_0}$ carries no charge initially and hence the voltage across it i.e. $\mathbf{V_h}$, was zero. $\mathbf{V_h}$ was connected to the

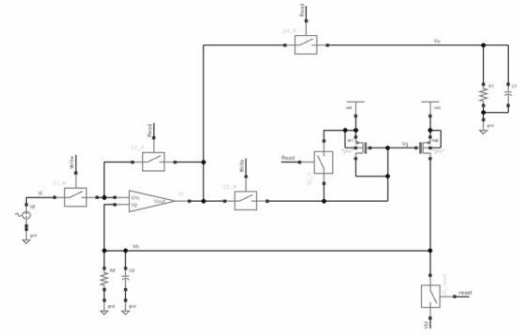

Fig. 2 *Schematic of a two-phase peak detector.*

positive input terminal of the amplifier, therefore $\mathbf{V_m} > \mathbf{V_h}$ resulted a sharp fall in the output voltage of the amplifier ($\mathbf{V_g}$) which turned on the current mirror (M0-M1) to charge $\mathbf{C_0}$ to make $\mathbf{V_h}$ same as $\mathbf{V_i}$. As $\mathbf{V_i}$ reached its peak voltage and stopped rising, output of the amplifier switched-off the current supply of the current mirror.

On the other hand, in the read phase S1_W and S2_W were switched off. S3_R, S4_R, and S5_R were kept ON to cut-off the input from the circuit. The peak value which was stored in $\mathbf{C_0}$ was read as the output voltage ($\mathbf{V_{out}}$) across load (R_1 and C_1), as the amplifier acts as buffer. The core amplifier of the PDH is shown in Fig 3.

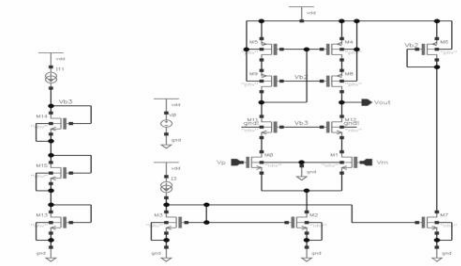

Fig. 3 *Schematic of the core amplifier.*

Results

Fig 4 shows the read and write phase of the PDH circuit. The sharp fall of the output voltage of the amplifier was obtained during write phase. The value of $\mathbf{V_h}$ was slightly higher than the input peak due to offset of the amplifier. However, the same has been balanced out during read phase as shown in the Fig 4. The result was encouraging in respect of implementation of the PDH circuit using HV CMOS of SCL 0.18 µm CMOS technology.

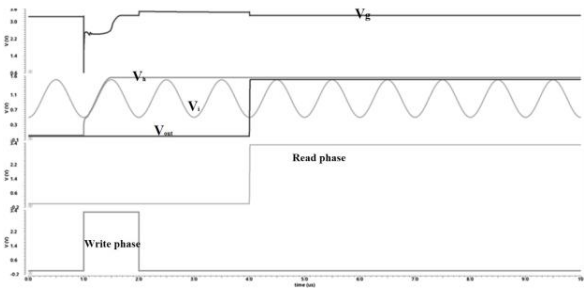

Fig. 4 *Output of the designed PDH.*

Conclusion

The PDH circuit along with the readout will be implemented in ASIC for fabrication after the implementation of a proto-type independent digital DAQ for final testing.

References

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