# Optimization methodology of high speed transceivers for interfaces in HEP Experiments

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## Introduction

The plan of the data acquisition (DAQ) scheme in High Energy Physics (HEP) experiments comprises of information transfer from the front-end electronics (FEE) of the detectors placed in experimental cavern to the data storage via the FPGA based data processing units [1]. With major upgrades of the LHC experiments at CERN, the data transmission rates in the DAQ frameworks are expected to reach about few terrabytes per second within the following couple of years [2]. These high rates are normally connected with the increment in the high-frequency losses. It leads to distortion in the detected signal and deterioration of signal integrity. Thus, it is a challenge to minimize the bit error ratio (BER) and improve signal integrity for the increased data rates. To address these challenges, we have designed a methodology using the heuristic approach to optimize the parameters of high speed transceivers also known as multigigabit transceivers (MGT). The technique helps to achieve the improved performance at specified rates of transmission for data, trigger, timing and slow control information. In this paper, the optimization technique is implemented on a latest 20nm Intel Arria-10 FPGA. It is tested for the link rate of three high-speed communication protocols commonly used for data transmission in the HEP experiments. The robustness of the optimization technique has been tested with most stressed and transitional data conditions. The test results and the improvements in the metrics of signal integrity for different link speeds are presented and discussed.

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## Optimization methodology

To reduce the high frequency losses, the high-frequency components in the data stream are boosted up on every switching, using the digital pre-emphasis taps of the on-chip transceiver. In addition, the low frequency components are reduced. This technique helps to achieve the same amount of emphasis with less power dissipation. The exaggerations are overridden by the attenuation during transmission and allow for the signal to be recovered accurately. Intel Arria-10 development board has integrated reconfigurable transceiver architecture which incorporates additional circuitry in buffers for equalisation and pre-emphasis techniques. The transmitter of the embedded transceiver has five programmable drivers as shown in Figure 1.

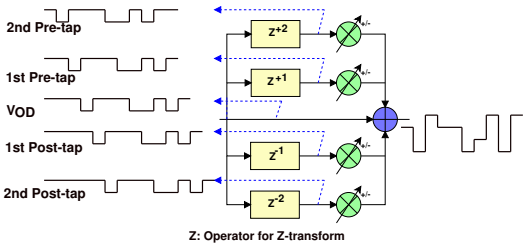


FIG. 1: Voltage output differential (VOD) and tunable pre-emphasis taps with flexible polarity in the embedded transceiver of FPGA.

Voltage output differential (VOD) controls the base amplitude. The four pre-emphasis taps are 1st pre-tap, 2nd pre-tap, 1st post-tap and 2nd post-tap. These taps also include polarity settings. The post taps are the causal taps and the pre-taps are the anti-causal taps. These multiple taps and choice of polarity handles the channel attenuating characteristics. Equalisation with DC gain and Variable

Gain Amplifier (VGA) is on the receiver side of the transceiver. The transceiver parameters has a large range of operating values. Hence to scan the system performance for every combination of the parameters is a time-consuming process. The proposed optimization method scans the full range of each transceiver parameter using the auto-sweep feature while the rest of the parameters are set at their Intel-default values. It records the best performing tap setting values for each transceiver parameter as indicated by eye parameters. The parameters cannot be declared as optimized until a stage of degradation in the signal integrity metrics from their peak values is observed. The degradation of metrics denotes the over-compensation and it marks the transition from the maxima of the transceiver parameters. The final **S** values with the best performing metrics is known as *Solution Space*.

## Results and discussion

Results are validated for the three different high speed optical links: 10 Gbps links, 4.8 Gbps Gigabit Transceiver (GBT) protocol and 9.6 Gbps TTC-PON protocol for use in trigger. With the application of the deduced solution space to the transceivers an improvement in the system performance is marked by two metrics of signal integrity viz. BER and Eye Diagram. The optimized transceiver parameters values, found from the proposed methodology for the targeted BER of $10^{-12}$ are plotted against the Intel-default set in the form of a multivariate kiviat diagram for the three link speeds as shown in Figure 2. It demonstrates a clear comparison of the individual parameters on each axis. The detailed results and improvement in signal integrity will be presented.

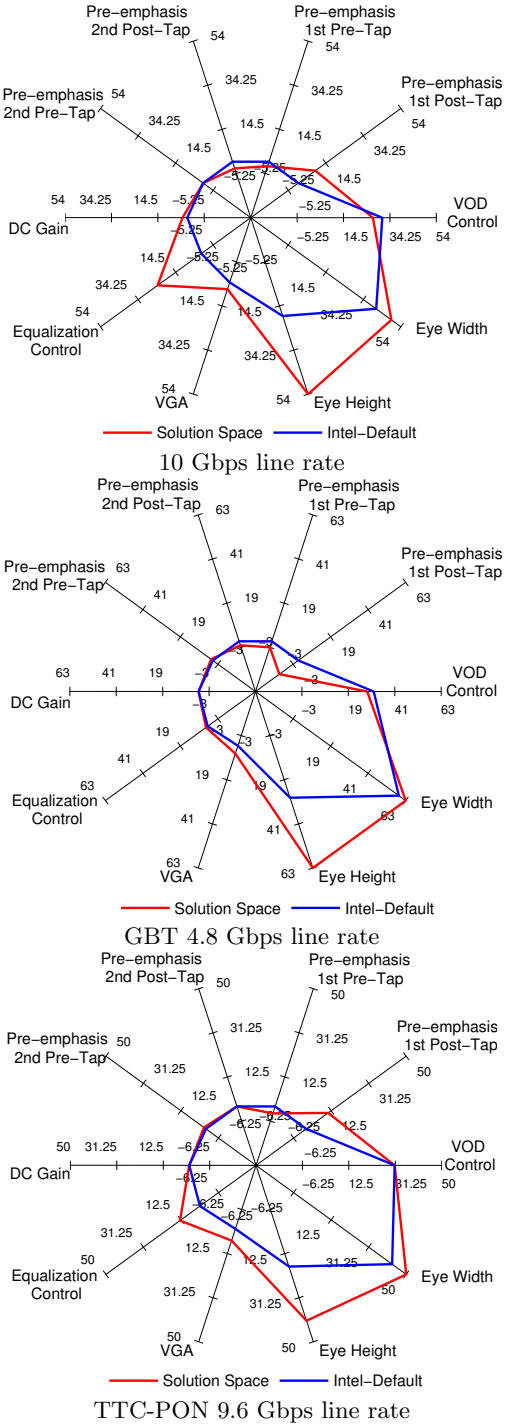


FIG. 2: Multivariate kiviat diagram showing the solution space and the Intel FPGA default values for the three link rates.

## References

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[2] P. Antonioli, A. Kluge, and W. Riegler (ALICE), Tech. Rep. CERN-LHCC-2013-019. ALICE-