Low volume production yield study of a BiCMOS frontend ASIC chipset for INO-ICAL RPC detector

Menka Sukhwani[1,2*], V.B.Chandratre[1,2], K Hari Prasad[1,2], Tushar Kesarkar[1], Megha Thomas[3]

[1]*Electronics Division, Bhabha Atomic Research Centre, Mumbai - 400085, INDIA*
[2]*Homi Bhabha National Institute, Mumbai-400094, INDIA*
[3] *Electronics Corporation of India Ltd., Mumbai-40028, INDIA.*
** email: menkat@barc.gov.in*

Introduction

This paper presents the low volume production yield study of a BiCMOS voltage-amplifier based frontend electronics (FEE) ASIC chipset, designed in the 0.35 μm SiGe BiCMOS technology. The FEE ASIC chipset is developed for the readout of ~ 3.7 million channels of the Resistive Plate Chamber (RPC) detector of the Iron Calorimeter (ICAL) experiment of the India based Neutrino Observatory (INO) [1]. This FEE chipset comprises a high speed, low power quad amplifier ASIC and an octal comparator ASIC.

This FEE ASIC chipset has met the readout requirements of the INO-ICAL RPC detector by exhibiting a detector efficiency of larger than 90% with prototype RPC detector of size 1 m x 2 m [2]. Therefore, this FEE chipset has been taken up for a low volume production run. In this run, 40,000 devices are fabricated comprising quad amplifier and octal comparator ASICs in a ratio of 2:1.

As the FEE ASIC chipset was packaged in QFN48, without die-level testing, in the low volume production run, it was required to perform an automated pre-assembly test to estimate its performance yield. The details of functional test requirements, automated test-jig configuration and the yield test results are described in the following sections.

Functional test requirements of the FEE chipset

Each channel of the quad voltage amplifier ASIC comprises three-stage fully differential voltage amplifier followed by a dynamically biased analog 50 Ω cable driver. Similarly, each channel of the octal comparator ASIC comprises a BiCMOS comparator and LVDS driver with a common threshold [3]. A multiplexed analog output is also provided in the comparator ASIC that can be accessed by manual control or through daisy chaining. The specifications of the FEE ASIC chipset are summarized in Table-1.

Table 1 Specifications of the FEE ASIC chipset

No of channels	Amplifier ASIC: 4 Comparator ASIC: 8
Amplifier rise time	1.2 ns
Amplifier gain	74
Input dynamic range	0.5 mV – 9 mV
LVDS output current	3.5 mA/channel
Overall timing precision	140 ps RMS
Power consumption	25 mW/channel
Power Supply	± 1.5 V

The parameters that need to be measured to perform the low volume production yield study of the FEE ASIC chipset involved,

i) Unloaded (without ASIC) DC test including bias points and supply current monitoring.
ii) Amplifier output profile test including measurement of rise-time, pulse height, base-line stability, overshoot/undershoot along with uniformity across amplifier channels.
iii) Comparator LVDS output compatibility test with a standard LVDS receiver and LVDS event rate stability test at a fixed threshold setting using a DAQ
iv) Daisy and manual readout test of multiplexed analog output of the comparator ASIC.

Automated test-jig configuration

In order to perform above performance tests on the blind packaged FEE ASICs from low volume production run, an automated test-jig was developed. The test-jig comprised QFN48 ZIF

socket based two independent test boards for the amplifier and comparator ASICs, respectively. These test boards received required pulse inputs from a 1 Gbps Arbitrary Waveform Generator. The amplifier output profile was analyzed through a mask test on the 1 GHz oscilloscope. This mask was defined as a pulse envelope within ± 5 % of the expected amplifier output considering amplifier gain, rise time, input pulse width and system noise. The comparator LVDS output was acquired through an FPGA based data acquisition module with LVDS receiver and a clocked pattern was used to test the daisy mode multiplexed analog readout. Further, a Switch Matrix based digital multimeter was sequentially interfaced to various bias points of the test board to ensure accurate operating conditions on continuous basis. All of these instruments along with the power supply module were interfaced to a central control unit through GPIB/LAN/PXI and were programmed/monitored through a LabView based GUI. The test-jig configuration is shown in Fig.1.

Test Results:

The low volume production yield tests of the FEE ASICs were performed on the randomly sampled 1000 devices among 40,000 devices. These tests resulted in a functional yield of 98%. Further, considering a tolerance margin of ±5%, the performance yield of the quad amplifier ASIC was measured to be 85% and of the octal comparator ASIC was 95%. It was observed that the performance of the FEE ASICs was mainly affected by the non-uniformity of the amplifier profile and LVDS event rate across the channels. The test results are summarized in Table 2.

Table 2: Test results of FEE ASIC yield study

Total no of tested devices	1000 (randomly sampled)
Functional yield	98%
Performance yield within ± 5 % tolerance margin	Amplifier: 85% Comparator: 95%

The tested FEE ASICs were used to develop 40 octal FEE modules that are tested with the prototype INO-ICAL detectors meeting the experimental requirements.

References

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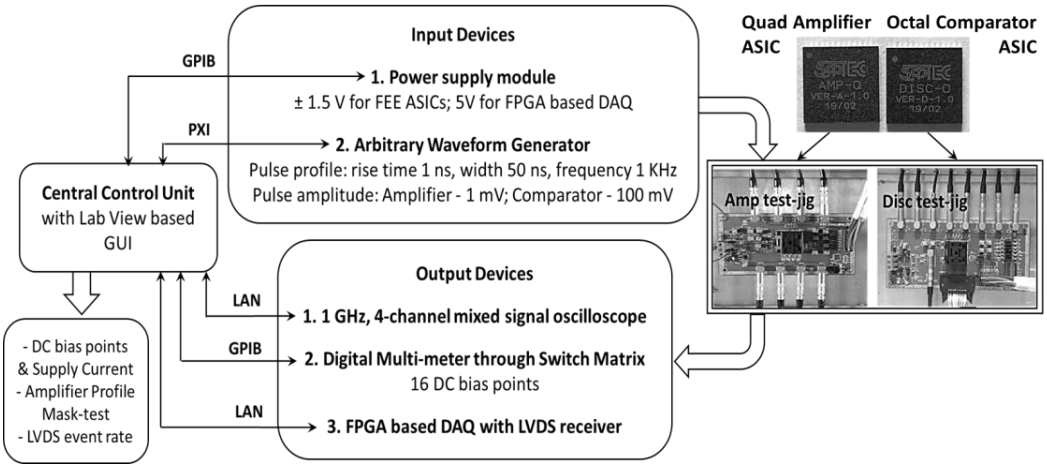

Fig. 1 Configuration of the automatic test-jig for low volume production yield test of the INO-ICAL FEE ASICs