Development of Multichannel Shaping and Timing ASIC for Charged Particle Detector Array

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Introduction

The Multichannel Charge Sensitive Amplifier (MCSA-16) module [1] using VECC001 ASIC has already been developed successfully for the front-end signal processing of silicon strip detectors used in Charge Particle Detector Array (CPDA) at VECC. A commercial shaping-cum-timing module is being used presently to process the CSA output further for spectroscopy application with VME based 13-bit ADC. The MSCA-16 module has been designed by introducing additional circuitry after the ASIC to match the output signal of the CSA as per the input requirements of the commercial module. This has introduced additional noise and power consumption to the MCSA-16 which could not be optimized after a certain level. All the effort of power and noise optimized design of the VECC001 ASIC goes in vain for using these type of heterogeneous systems. Moreover, the advantage of using ASIC in CPDA is its ability to couple itself just behind the detector within the vacuum chamber which reduces noise introduced from the cable capacitances. However, this advantage could not be availed while using such type of module in CPDA structure.

The development of an indigenous Multichannel Shaping and Timing ASIC has been undertaken to provide an efficient signal processing mechanism for the CPDA. The aim of these developments is to design independent signal processing chain of CPDA or any other similar facilities utilizing these ASICs. After the success of CSA ASIC, the Shaping and Timing ASIC has been designed successfully and will be used in conjunction with the CSA ASIC. The schematic design of the single channel has been described in the subsequent section followed by layout, verification and tape-out details. The post layout performance analysis which depicts the actual performance of the ASIC after fabrication has also been elaborated with performance metrics in the following sections.

Design of Shaping & Timing Channel

The single-channel block diagram of the schematic design is shown in Fig. 1.

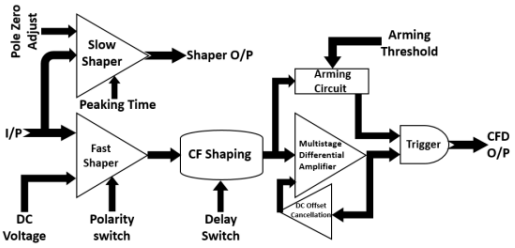


Fig. 1: Single channel block diagram of Shaping and Timing ASIC

The mixed-signal design has two sections. The first section consists of a fifth-order slow shaper is for energy measurement. Its linearity deviation is less than 1 % and has selectable shaping time of 0.5/1 µs with external pole-zero compensation option. The other section is designed for generation of gating signal required during the spectroscopic application. It consists of a fast shaper and a timing discriminator. This timing discriminator is designed using constant fraction discrimination method [2]. The timing circuit can cater to positive and negative inputs, and has an option to switch delay time in CFD as well. This discriminator design has achieved 200 ps time resolution as per the requirement of the CPDA.

Layout, Verification and Tape-out

The schematic design of a single channel of Shaping and Timing ASIC has been successfully tested with a test-bench and layout for the same for the mask fabrication has been undertaken. Fig. 2 shows slow shaper and discriminator layout of the ASIC. The layout is designed after

DRC and LVS check at each stage for successful fabrication. The parasitic extraction is carried out to check the realistic result in the post layout simulation. The corner analysis for process, temperature and supply voltage variation has been carried out followed by Monte-Carlo analysis and it is found that the result is within the limit of design specifications and ready for final tape-out after integration of sixteen channel.

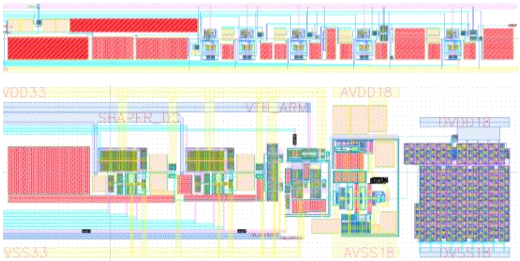


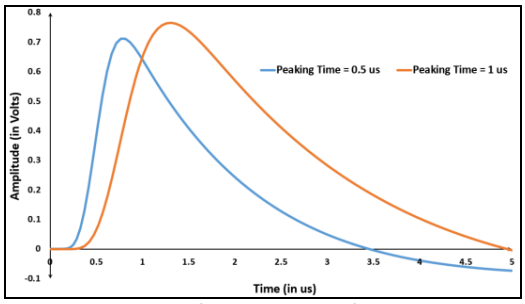
Fig. 2: Slow Shaper (above) and Discriminator (below) layout of the ASIC

Post Layout Simulation of Single Channel Tape-out

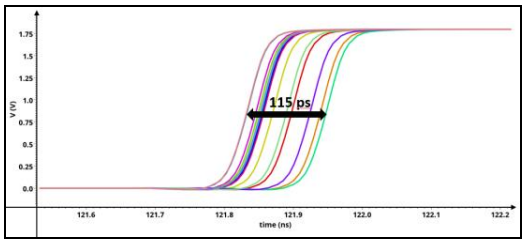
The result of post-layout simulation is shown in Fig. 3. It is observed that the shaping time matches the design specifications of 0.5/1 µs. The tail of the shaper output is kept in over-damped condition to increase linearity, however, it returns to zero within 10 µs which is enough to handle the count rate of the application. The trigger signal is also shown in Fig. 3(b) which has an amplitude walk of 115 ps for 1:25 ratio of peak input amplitude having a rise time of 25 ns. All other specifications of the ASIC after post-layout simulation are as per the requirement of the application.

Conclusion

A single channel of Shaping and Timing ASIC has been designed successfully and will be sent for fabrication after chip-finishing to Semiconductor Laboratory, Chandigarh. This ASIC will be packaged in CQFP-120 package and functional testing will be carried out. A generalized NIM module similar to the commercial module mentioned above will be developed using this ASIC for self-reliance and as an import substitute.



(a) Output of Slow Shaper for 0.5 µs and 1 µs Peaking Time



(b) Amplitude Walk of Discriminator for 1:25 Ratio of Peak Input Amplitude

Fig. 3: Results of Post-layout Simulation

References

[1] M. K. Jha et al " Development and characterization of MCSA-16 module using VECC-001 multichannel CSA ASIC for in-house application " , Proceedings of the DAE Symposium on Nuclear Physics , 2022 (this conference)

[2] M. L. Simpson, G. R. Young, R. G. Jackson and M. Xu, "A monolithic, constant-fraction discriminator using distributed R-C delay line shaping," in IEEE Transactions on Nuclear Science, vol. 43, no. 3, pp. 1695-1699, June 1996, doi: 10.1109/23.507173.