Design and Development of the FPGA based Data Acquisition for the Muon Tomography system

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Introduction

The Muon Tomography system at VECC Kolkata, uses the layered assembly of the bakelite based Resistive Plate Chambers (RPCs) as detectors to capture the passage of muons[1]. RPCs generate signals when muons interact and ionize the gas inside the detector chamber. The assembly detects the scattering of the cosmic muons passing through an object with high atomic number (Z) placed between the detector stack. The data from the detector assembly are used to recreate the image of an object's structure[2]. Here, we present the design and development of the FPGA-based Data Acquisition (DAQ) for the Muon Tomography system.

System overview and the Design architecture

Custom designed front end electronics (FEE) board receives the data from the RPC detector. The developed DAQ receives the data from the multiple FEE boards kept near the detector. The FPGA based DAQ multiplexes and transfers the data to the back-end computing servers. For reliable transmission; low voltage differential signals (LVDS) are used to transmit data over long distances from the FEE near the detectors to the DAQ located far from the detectors. In this regard, the development consists of two parts hardware and the firmware.

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Hardware Design

A customized FPGA Mezzanine Card (FMC) compatible with Kintex-7 based KC705 FPGA board from AMD is designed and developed [3]. The designed mezzanine module is optimized to provide the physical interface to multiple LVDS channels for FPGA fanout. Mezzanine card accesses the LVDS pulses from the FEE via the patch-bus cables and fed it to the KC705 FPGA card through the FMC high pin count (FMC-HPC) connector. The designed FMC card as shown in Figure 1, consists of 80 no. of LVDS differential

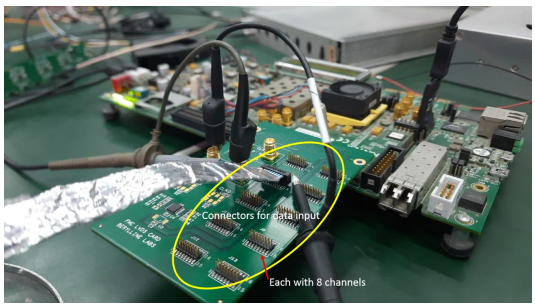

FIG. 1: Data input via 16 pin connector grouped into 08 no. LVDS channels. It is routed to FPGA through the mezzanine board.

pairs as external inputs, grouped in pairs, each with 8 no. of LVDS channels. It has 10 no. of 16 pin male connectors with 02 rows and 0.05" pitch for interfacing with external LVDS inputs from the FEE. Total 56 no. of LVDS differential pairs are used for the tests. The FMC card also has the provision for the external clocks as input to the FPGA. The challenge in the design to synchronize the transit time of the differential signals is achieved by

matching the copper length of the traces on the PCB with serpentine routing as shown in Figure 2. The technology is then coupled with

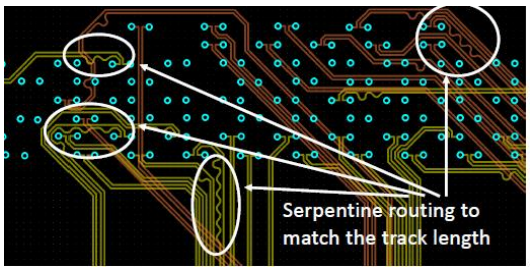

FIG. 2: Routing to match the track lengths.

advanced design rules and a dedicated routing mode to support differential pairs. Differential pairs are phase matched to keep the signals equal and opposite for as much of the transit time as possible. Traces from the FMC-HPC connector to the 2 row, 0.050 inch pitch, 16-pin connector are length-matched signal pairs. The data from the designed card is routed to the FPGA for further processing through the plugged in FMC-HPC connector. Provision is kept to connect total 10 no. of FEE boards to the developed card through the twisted pair patch buses. The developed PCB is of size 62.5mm x 96.2mm and 1.8mm thick.

Firmware and Software Development

The acquisition firmware is designed in VHDL hardware language. The P-N pair signal from the differential LVDS channels are mapped in the unified constraint file using the differential buffer (IBUFDS) on the FPGA input. The output from the IBUFDS is mapped to the FPGA signal and grouped to transmit to the PC using the UART serial communication at a baud rate of 9600(bits/sec) in the Xilinx-ise tool. A state machine is designed and implemented to capture the data simultaneously from the 08 no. of FEE patch buses on the 8-bit UART serial line. The data received at the PC is captured using the python interpreter and plotted channel wise.

Tests and Summary

FPGA setup is initially tested with NIM pulse generator as the data input along with an attenuator to maintain the compatible voltage level swing range. For validation of functionality; the developed DAQ is also tested in the coincidence setup with RPC detector and scintillators for muon tomography. The trigger for this setup is generated using the big and small paddle scintillators as shown in Figure 3 and the resulting cosmic data is captured for subsequent analysis. The results from the designed DAQ will be presented. The applicability of the developed DAQ is not only limited to particle physics; the customized design also fits well for industry and commercial applications like medical imaging and future experiments.

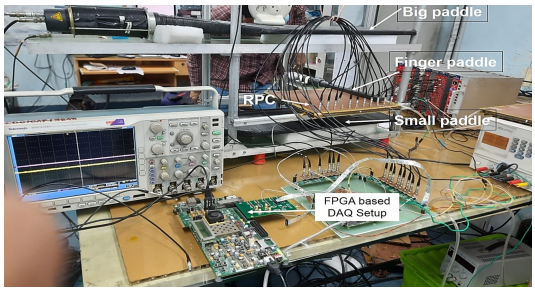

FIG. 3: Experimental Test setup with designed FMC card mounted on Kintex-7 FPGA and detector as RPC.

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