Prototype 2-Channel 1GSPS digitization system for qubit state measurements

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Introduction

A fundamental setup to measure quantum interaction is a system consisting a qubit and a cavity under controlled environmental conditions [1]. This system is crucial component in superconducting quantum computing as the cavity is electromagnetically coupled to the qubit, forming a system. The Qubit induces a state dependent frequency shift of cavity. Therefore, the natural way to detect the state of the qubit is to measure the phase shift across the cavity. This can be done by using homodyne measurement [2].

To carry out qubit state measurement, a stimulus pulse generated from I and Q pulses as shown in figure 1 will excite the qubit, causing it to rotate on the Bloch sphere. As the qubit stimulus frequency is swept, the qubit is increasingly excited. After the qubit stimulus pulse, a measurement pulse is given [3]. The response of the qubit to this measurement pulse travels out of the dilution refrigerator, carrying information about the state of the qubit via its shape or phase.

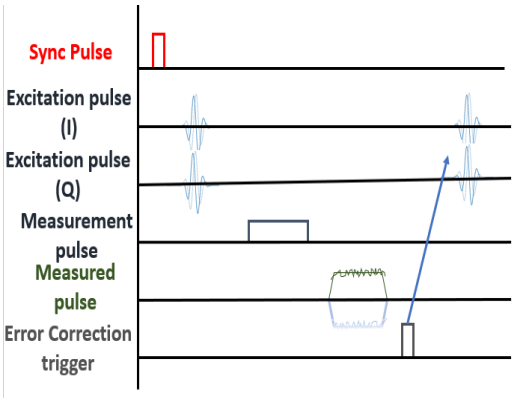

Fig.**1** Sequence Diagram for Qubit state measurement.

To detect this phase difference between input signal and the output signal, a high speed DAQ system is required [4].

In this paper a two-channel prototype DAQ system for reading the state of Qubit, by acquiring measurement pulse and analyzing the phase shift of acquired pulse, is developed. This developed FPGA based system performs digitization at a sampling rate of 983.04 MHz.

Hardware Architecture

The two-channel prototype DAQ system incorporates a 14-bit, Dual analog to digital convertor (ADC) with a sampling rate of 1GSPS, connected via a JESD204B interface to a System on Chip board (SoC). A clock module generates the clock for ADC sampling clock and device clock for SoC board.

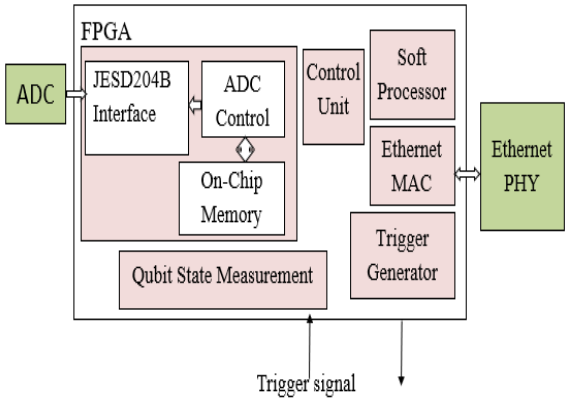

Fig. 2 Hardware architecture diagram.

The ADC is interfaced with FPGA using high speed serial interface JESD204B as shown in figure 2.

A VHDL code is implemented on System on chip (SoC) to acquire ADC data. This Acquired data is processed at a programmable delay from onset of Trigger. All parameter like, width of

profile data to be transmitted, delay from trigger for start of processing/Averaging, time duration for which averaging of the data needs to be carried out is configurable by developed user software. Qubit state measurement block of the VHDL code can estimate the phase of measurement pulse using these user's configurable parameter and can perform demodulation.

To facilitate the acquired data transfer for analysis to computer over network a 1 gigabit ethernet interface is also implemented in VHDL code.

Experimental Setup

In order to evaluate the performance of developed prototype system, the system is tested with arbitrary waveform generator. All the hardware components were interconnected as shown in Figure 3. A measurement pulse sine wave was given as input to channel A of the system. A gaussian modulated sine wave of pulse width 300 nanoseconds, amplitude 0.14 Vp-p and frequency 320 MHz, the simulated excitation pulse was given as input to channel B of the system. The clock module was setting the sampling clock to 983.04Mhz and device clock to 245.76 MHz. The input signals were sampled by the ADC. Sampled input data was transferred to FPGA using serial interface at the lane rate of 5Gbps. Acquired data at FPGA side was first stored in a buffer and processed at a clock rate of 245.75 Mhz. Stored data was formatted into Ethernet packets and transmitted over an Ethernet link at 1 Gbps. A user interface was also developed to plot the acquired data.

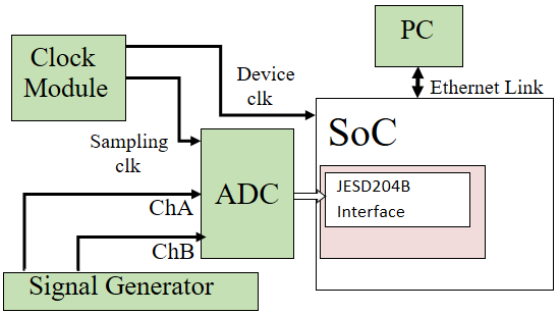

Fig. 3 Complete setup for prototype testing.

Result and Future scope

As show in figure 4, Input measuring pulse a digitized sine wave, channel A input of the prototype system is plotted above.

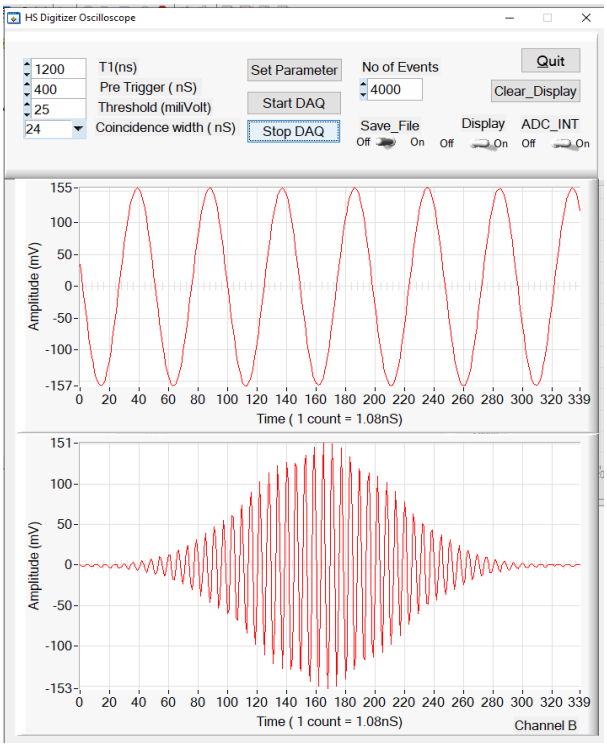

Fig. 4 User interface software plot of acquired data by the prototype system.

A digitized gaussian modulated sine wave as excitation pulse, channel B input of the prototype system is plotted below. Sampling interval here in the plot is 1.018 ns.

References

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