Evolution and implementation of precision time interval measurement techniques in ASIC and FPGA technologies

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Introduction

In modern High Energy Physics (HEP) experiments, with the rapid development in detector technologies, the timing resolutions are improving to sub 100 ps, along with the increase in the number of measurement channels and functionality. These requirements increase the complexity of the readout electronics in terms of time resolution, number of channels, space, and power consumption. These requirements are well supported by the advancements in integrated circuit technology in the form of Application Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). In the research work presented in this thesis, these requirements are addressed by evolving and implementing various precise time interval measurement methods in ASIC and FPGA technologies. Apart from HEP experiments, precise Time Interval (TI) measurement is also required in other applications, such as nuclear physics experiments, time-of-flight mass spectroscopy, laser range finding, ultrasonic measurements, and tomography experiments. These experimental requirements form the objective of implementing a precise, multi-channel, multi-hit, TI measurement system having < 200 ps resolution and 10's µs of range.

The precision TI measurement is often realized using time-to-digital converters (TDCs). Various techniques like delay line, Vernier oscillator, and multi-phase clock (MPC) are used to realize high-resolution TDC. These methods can be implemented in either ASIC or FPGA technologies.

Challenges

This research work contributes to the field of precision TI measurement by addressing the following challenging aspects in implementing the TDC in ASIC and FPGA technologies: obtaining the resolution beyond minimum available gate delay; incorporating multiple hits; overcoming the limitations due to unpredictable place & routes delays in FPGA; obtaining consistent performance across channels; and mitigating the effects due to process, voltage, and temperature (PVT) variations. In TDCs with a large number of channels, arriving at the optimum values of logic resources, clock frequency, power consumption, and meeting the timing uniformity across channels in a given device is a significant challenge to address.

Various TDCs in ASIC and FPGA technologies are implemented as part of this research work by overcoming these challenges.

Multi-channel, Multi-hit ASIC TDC

In this research work, a multi-hit, multi-channel, multi-mode TDC ASIC is implemented in 0.35 µm commercial CMOS technology, facilitating future integration with the FEE ASIC. The critical aspects addressed in this work are achieving sub-gate delay TDC resolution while accommodating multiple channels and hits, with low pulse pair resolution. The TDC using a Vernier technique is implemented to address these aspects. The ASIC has eight channels, each capable of handling four hits: a pair of rising and falling edges. The ASIC has a unique in-built calibration for each channel to mitigate the effects due to PVT variations. The TDC has a selectable dynamic range (4 µs, 16 µs, 32 µs, & 64 µs), multiple modes, serial and parallel interfaces to make this ASIC suitable for a large number of applications. The TDC ASIC [1] has a least significant bit (LSB) resolution of about 120 ps and precision (σ) of < 70 ps across the channels.

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Multi-channel FPGA based TDC

In this research work, subsequent to the ASIC-based TDC implementation, an FPGA based TDC is developed to integrate the TDC with system processor, trigger logic in a single FPGA and Ethernet to ease the space and power requirements of the DAQ. The FPGA-based TDCs have benefited from the direct availability of resources like carry chains, clock managers, memory blocks, and inbuilt customizable I/O elements. However, these TDCs have to address the challenges like lack of direct control over the delays, unpredictable place and route delays, and careful allocation of resources.

This work implements a multi-channel TDC in AMD Spartan-6 FPGA using the tapped delay line (TDL) interpolation technique to cater to the triggered DAQ requirements. The technique is evolved further to implement the 33-channel TDC using the FPGA carry chains. The highlights of this implementation are as follows: This work features a novel bit-latching scheme to capture the TDC data. It also has a low resource-consuming calibration mechanism to achieve stable resolution under PVT variations. The TDC [2] has an LSB resolution of about 72.4 ps across the channels, a dynamic range of 20 µs, and a power consumption of 12.12 mW per channel. The TDC has a low channel-to-channel variation in the precision of approximately 3 ps.

The 33-channel TDC implementation was followed by the implementation of a high-density TDC (129- channel) in an FPGA to cater to the trigger-less DAQ requirements. The 129-channel TDC using the TDL interpolation technique is implemented in the Spartan-6 FPGA. The highlights of this implementation are as follows: In this work, a dual-hit TDC technique, capable of capturing dual hits using a single channel, is developed. An optimum resource and power-aware design approach are developed to implement TDC with a large number of channels having consistent performance in all 129 channels. An approach to properly partition the channels in a given FPGA is developed along with semi-automatic placement scripts to reduce the time and effort in placing this high-density TDC. All the TDC channels have an inbuilt, in system calibration mechanism to calibrate the TDC against PVT variations. This work resulted in a 129-channel TDC [3], having a resolution of 84.4 ps ± 2.5 ps, a precision of 42 ps (0.49 LSB) to 58 ps (0.68 LSB) as shown in Fig. 1, good linearity with differential Non-linearity (DNL): ± 0.45 LSB, integral non-linearity (INL): [-0.49, 0.84] LSB across the dynamic range of 40 µs, and power consumption of 7 mW/channel.

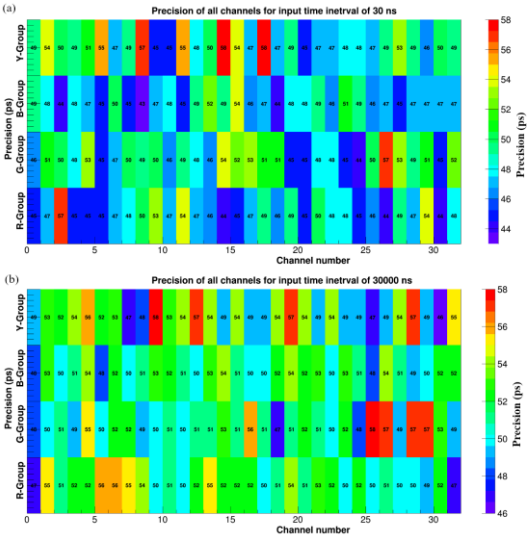

Fig. 1 Precision measurements at (a) 30 ns and (b) 30 µs time inputs. TDC channels are divided in 4 groups (R, B, G and Y) having 32-channels per group.

In summary, this work resulted in an implementation of sub 100 ps resolution, multi-channel, multi-hit TDCs in ASIC and FPGAs.

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